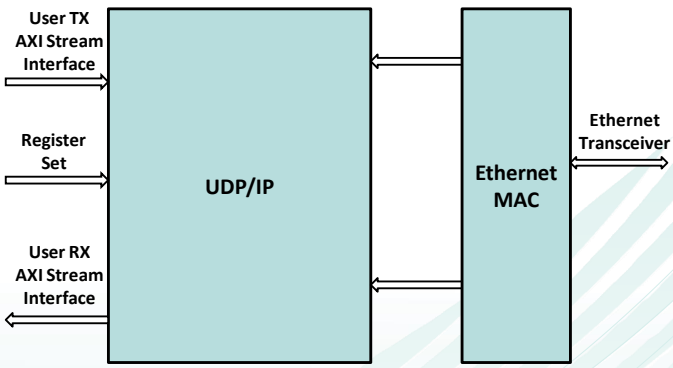
FPGA IP CORE

iW UDP/IP



The UDP/IP Hardware protocol stack offloads UDP encapsulation task from the host processor enabling media streaming with speed up to 40G even in a processor less non-SoC designs, making it ideal for any standalone operation. This IP core provides an effective infrastructure to implement high-speed communication between the FPGA and other network devices. It supports easy to use AXI streams on the FPGA to connect to the network devices.

Highlights

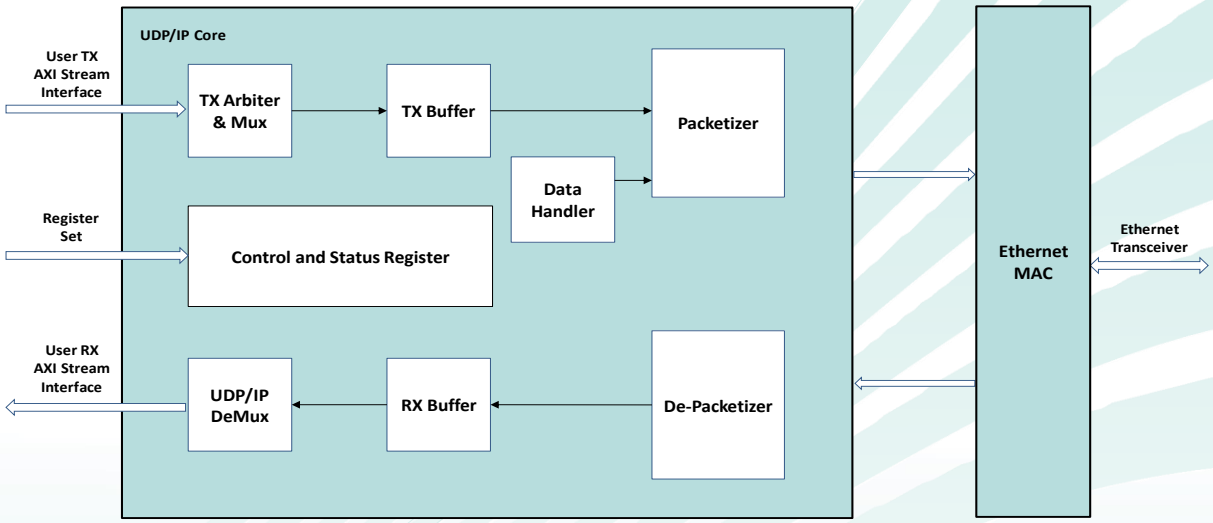
- Bring full UDP/IP connectivity to FPGAs even if no CPU is available
- Offload UDP/IP processing into programmable logic
- Enable media streaming with speed up to 40G
- Offers a configurable number of UDP transmit and receive channels
- The core can be easily mapped with different programmable devices, such as Xilinx, Intel, or with any ASIC technology.

Features

- Easy integration with 1G, 10G, and 40G Ethernet MAC
- Configurable number of UDP Transmit & Receive channels from 1 to 32
- IPV4 support without packet fragmentation
- Supports GMII/RGMII/SGMII/XGMII/XLGRMII interfaces
- Echo-Request & Reply messages (“ping”) of the Internet Control Message Protocol (ICMP) used to test network connectivity
- Address Resolution Protocol (ARP) for proper functioning over the internet
- UDP & IP checksum generation and validation support
- 32bit, 64bit, and 128bit AXI stream interface for transmission & reception of user data and 32bit AXI4-Lite interface for handling control and status registers
- Configurable buffer sizes for easy SoC integration
- Supports optional Dynamic Host Configuration Protocol (DHCP) client

iWave

iW UDP/IP block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site
- Non-Transferable: Multi Project/Product Netlist License – Single Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site
- Non-Transferable: Multi Project/Product RTL Source Code License – Single Site

Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave System Technologies, established in 1999, focuses on Product Engineering Services involving Embedded Hardware, Software & FPGA. The company designs and develops cutting edge products and provides the FPGA programable design solutions. iWave has been a leader in providing the robust and comprehensive IP cores and turnkey FPGA design services.

iW UDP/IP Core
The IP can be ordered online from the iWave Website https://www.iwavesystems.com/product/udp-ip-core/
Or from our Local Partners in your region https://www.iwavesystems.com/business-partners/

iWave Systems Tech. Pvt. Ltd.,
7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore-560076, India.
Ph:+91-80-26683700, 26786245
Email: mktg@iwavesystems.com
www.iwavesystems.com

iWave Japan, Inc.
8F-B, Kannai Sumiyoshi Building,
3-29, Sumiyoshi-cho, Naka-ku,
Yokohama, Kanagawa, Japan.
Ph: +81-45-227-7626
Email: info@iwavejapan.co.jp
www.iwavejapan.co.jp

iWave Europe
Stolwijkstraat 33,
3079 DD Rotterdam,
The Netherlands
Ph: +31 10 28403383
Email: info@iwavesystems.eu

iWave USA:
1692 Westmont Ave.,
Campbell, CA95008
USA
Ph: 408-206-5958
Email: info@iwavesystems.us