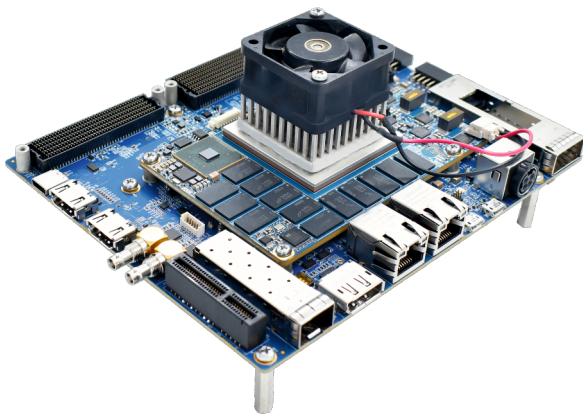




Virtex UltraScale+ FPGA SOM Development Platform



iW-RainboW-G47D Quick Start Guide

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Introduction

Quick Start Guide (QSG)

This Quick Start Guide (QSG) is designed for users to quickly understand the iW-RainboW-G47D-Virtex UltraScale+ FPGA SOM Development Platform and start the evaluation. It provides the instructions for setting-up the Development Platform from the packed box.

Development Platform Description

The iW-RainboW-G47D Virtex UltraScale+ FPGA SOM Development platform incorporates with iWave's Virtex UltraScale+ FPGA based SOM and Ultra High Performance carrier board with all necessary interface connectors for developing an embedded application based on Xilinx Virtex UltraScale+ FPGA.

Some Key Features of the Board Include:

- Virtex US+ FPGA SoC with 3780K Logic Cells
- Layerscape (LS1021A) CPU with dual-core Cortex-A7
- Dual 4GB PL DDR4 for FPGA
- 128MB QSPI Flash (FPGA)
- 2GB DDR4 for CPU
- 256MB NOR Flash (CPU)
- USB 3.0 Type-C & USB 2.0 OTG Port.
- PCIe x1 Port.
- Gigabit Ethernet RJ45 Magjack
- QSFP+ and SFP+ Connectors
- HDMI IN/OUT
- SDI IN/OUT
- 12 Pin PMOD Connectors
- Firefly Connector
- FMC+ and FMC HPC Connectors

Safety

Environmental Compliance

iW-RainboW-G47D-Virtex UltraScale+ FPGA SOM Development Platform is designed by using RoHS and REACH compliant components and manufactured on lead free production process.



ESD Protection

This development platform is ESD sensitive. Handle the product only in accordance with the installation instructions given in the manual. Therefore ESD precautions should be taken care during transport and handling.



Must use a ESD ground strap or other grounded source before unpacking or handling the hardware.

Product Disposal

Check the local regulations for disposal of electronic products before disposing.



Quick Start Steps

Step 1 - Unpacking

Remove the Development platform from anti-static cover and place it above the ESD free area. Use anti-static pad/mat with proper grounding to place the Development Platform. Don't touch inside surface of the circuit board.

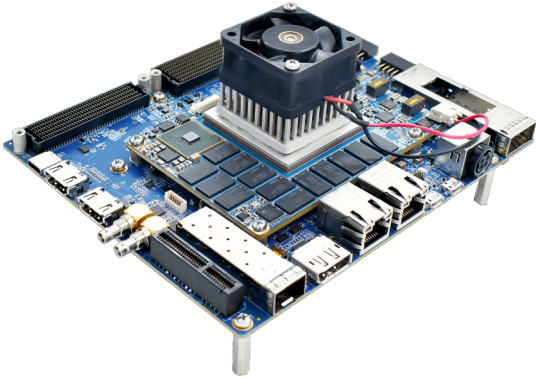
Avoid using board in extreme dust, humidity and temperature conditions. Also this development platform is not water proof. Keep away from wet surface.



Package Box

Step 2 - What's Inside The Box ?

Make sure that, below deliverables are received without any physical damage.



Development Platform



12V,14A Power Supply



USB OTG Cable

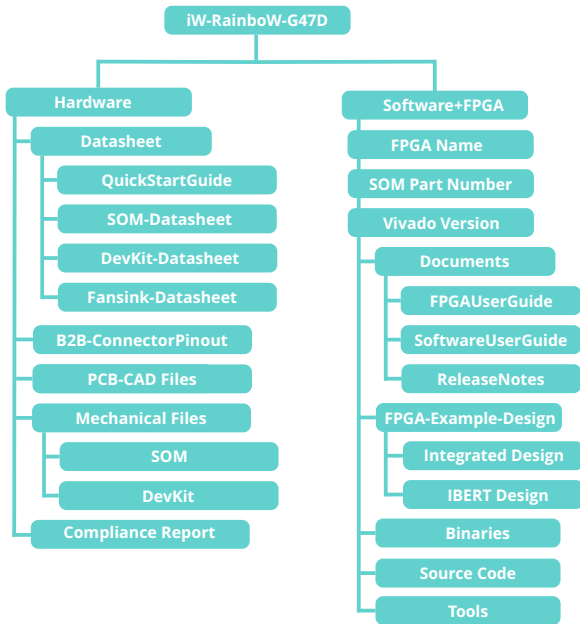


JTAG Cable

Step 3 - Download FTP Contents

All the technical resources of iW-RainboW-G47D Virtex UltraScale+ FPGA SOM Development platform is available in iWave FTP server.

FTP Folder Structure



Step 4- Read Documents

Before moving to next step, one must go through all the documents including Hardware Datasheets and get familiar about iW-RainboW-G47D Virtex UltraScale+ FPGA SOM Development platform.

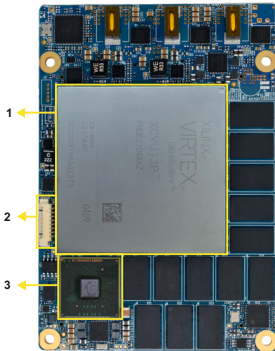
Development Platform Documents:

- Quick Start Guide (This document)
- SOM Datasheet
- DevKit Datasheet
- Release Notes
- Software User Guide
- FPGA User Guide



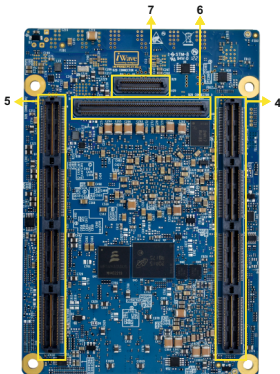
Step 5 -Quick View-SOM

TOP View



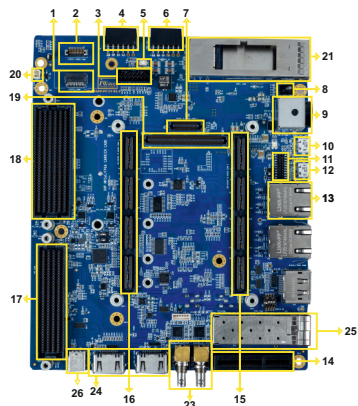
1. Virtex UltraScale+ FPGA SoC
2. PMIC Programming Header
3. LS1021A Layerscape CPU
4. Board to Board connector 1
5. Board to Board connector 2
6. Board to Board connector 3
7. Board to Board connector 4

BOTTOM View



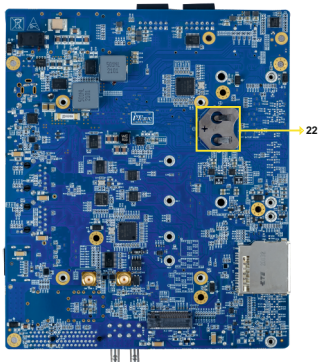
Step 6 - Quick View-Carrier Board

TOP View



01. FireFly Connector
02. FireFly Power Connector
03. JTAG Connector
04. PMOD Connector 2
05. Reset Switch
06. PMOD Connector 1
07. Board to Board Connector 4
08. Power ON/OFF Switch
09. Power Connector
10. Debug UART Connector
11. 20 Pin GPIO Header
12. USB 2.0 OTG Connector
13. Gigabit Ethernet Magjack
14. PCIe1 Connector
15. Board to Board Connector 2
16. Board to Board Connector 1
17. FMC Connector
18. FMC+ Connector
19. Board to Board Connector 3
20. 12V Fan Header
21. QSFP+ Connector
22. RTC Battery Holder
23. SDI IN/OUT
24. HDMI IN/OUT
25. SFP+ Connector
26. USB 3.0 Type-C Connector

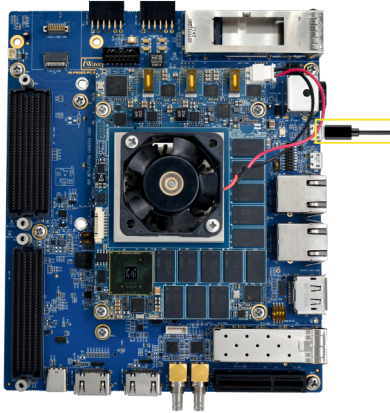
BOTTOM View



Note: Connectors which are not highlighted is not supported by the Virtex UltraScale+ FPGA Development Kit

Step 7 - Debug Port Setting

Connect TypeA end of USB cable to PC and MicroB end of USB cable to Development platform's Debug USB MicroAB Connector (J13) as shown below.



Install the driver for Debug Port in Host PC/Laptop using the below link.

<https://ftdichip.com/products/ft232rq/>

Setup the Debug Terminal parameters.

Baud Rate : 115200

Data bits : 8

Parity : None

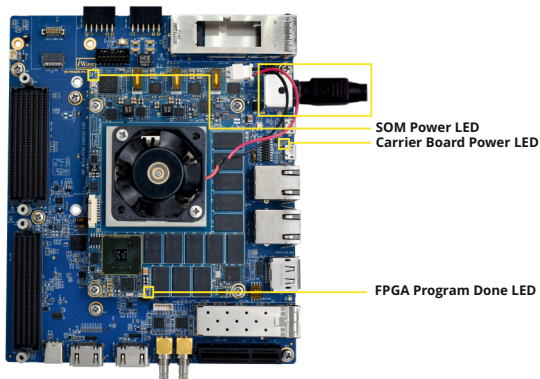
Stop Bits : 1

Flow Control : None

Step 8 - Power-ON the Development Platform

Connect the 12V power supply plug to the power connector (J10) of the Development platform as shown below and switch ON the power supply.

Once power is applied to the Development platform, the power LEDs in Virtex UltraScale+ FPGA SOM and Ultra High Speed Carrier Board will glow as shown in the below image.



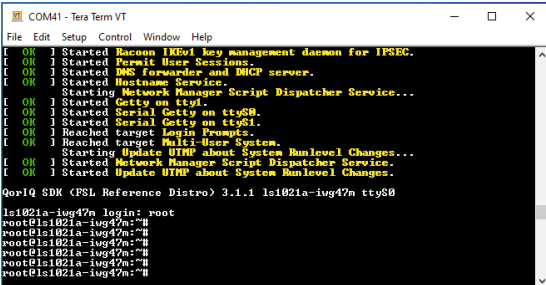
Warning:

1. Do not try to connect any other power supply other than supplied along with the Development platform.
2. Do not plug or remove the Virtex UltraScale+ FPGA SOM from carrier board with live power.
3. Contact iWave if any LEDs are not glowing

Step 9 - Test Environment setup

Once power is applied to the Development Platform as explained in the previous section, boot messages being displayed in the debug terminal of the PC/Laptop which is connected to the Development platform. Press any key in terminal immediately to see the command prompt of the Boot loader or wait until OS boots.

After OS boots, Login prompt being displayed in the debug terminal.

A screenshot of a terminal window titled "COM41 - Tera Term VT". The terminal displays a series of boot messages in a yellow font on a black background, including "Started Raccoon IKEv1 key management daemon for IPSEC.", "Started Permit User Sessions.", "Started DNS forwarder and DHCP server.", "Started Hostname Service.", "Starting Network Manager Script Dispatcher Service...", "Started Getty on ttyL", "Started Serial Getty on ttyS0.", "Started Serial Getty on ttyS1.", "Reached target Login Prompts.", "Reached target Multi-User System.", "Starting Update UTMP about System Runlevel Changes...", "Started Network Manager Script Dispatcher Service.", and "Started Update UTMP about System Runlevel Changes.". Below the messages, the terminal shows the QorIQ SDK (FSL Reference Distro) 3.1.1 ls1021a-iwg47n ttyS0 login prompt, followed by several "root@ls1021a-iwg47n:~#" prompts.

Debug Terminal

Heat Sink

Heat Sink Integration

iW-RainboW-G47D Virtex UltraScale+ FPGA SOM Development platform comes with Heat Sink + Fan mounted on SOM. Makesure to power up the platform only with Heatsink+Fan attached.

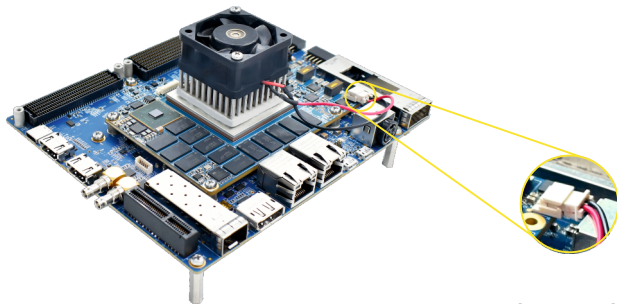
Below is the Heatsink+Fan integration procedure for reference.



Heatsink + Fan



Peel off Thermal pad sticker



Fix the heatsink in to SOM

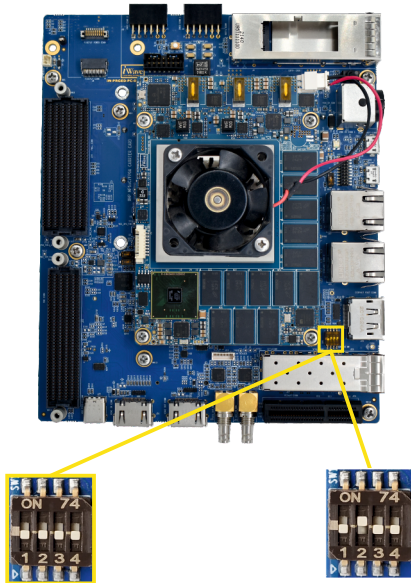
Connect the Fan cable to SOM Fan Header

JTAG

JTAG Connection

iW-RainboW-G47D Virtex UltraScale+ FPGA SOM Development platform Support JTAG interface in Carrier Board for FPGA and CPU Programming.

In the carrier board Config Switch (SW6.2) is provided for selecting the JTAG device between FPGA and CPU.



FPGA as JTAG Device

CPU as JTAG Device

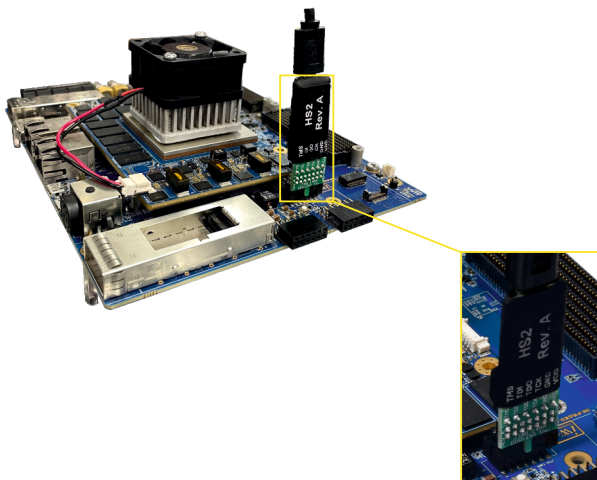
FPGA JTAG Connection to Carrier Board :

After changing Config switch and selecting the JTAG device as FPGA, Power on the board connect the JTAG cable to the carrier board as shown below.

Example JTAG Cable which is tested with this Platform is mentioned below.

JTAG-HS2 Programming Cable

Part Number: 410-249 from Digilent



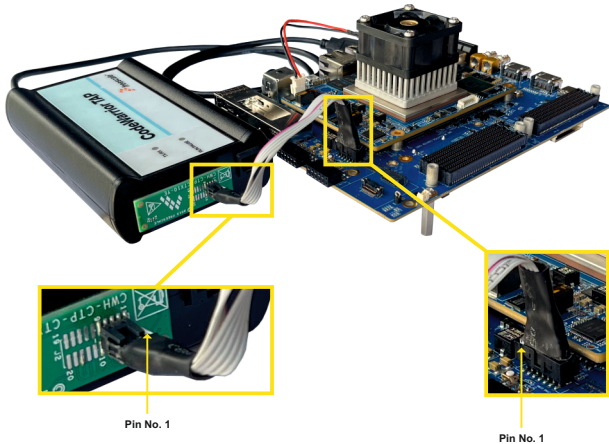
CPU JTAG Connection to Carrier Board :

After changing Config switch and selecting the JTAG device as CPU, connect the CodeWarrior® TAP to carrier board via custom made JTAG cable provided from iWave.

Connect the CodeWarrior® TAP to the PC through USB and Power on the board.

For further details regarding CodeWarrior® TAP, visit the below link:

https://www.nxp.com/design/software/development-software/codewarrior-development-tools/run-control-devices/codewarrior-tap:CW_TAP



iWave's Other Products

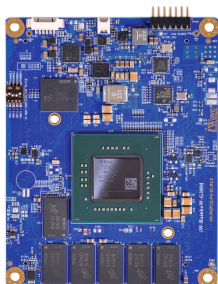


Product Name: Zynq UltraScale+ MPSoC (ZU5/ZU4/ZU3/ZU2) SBC

Processor: Xilinx's Zynq US+ MPSoC (2/3/4/5-EV/EG/CG)

RAM: 8GB PS DDR4* & 4GB PL DDR4*

Application: AI/ML, Industrial IoT, Human Machine Interface, Advanced Driver Assistance Systems.

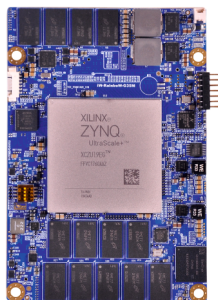


Product Name: Zynq US+ MPSoC (4/5/7-EV/EG/CG) SOM

Processor: Xilinx's Zynq US+ MPSoC (4/5/7-EV/EG/CG)

RAM: 4GB PS DDR4*
1GB PL DDR4*

Application: Industrial Motor Control & IoT, Sensor Fusion, ADAS/Embedded Vision, Data Center, Medical Endoscopy



Product Name: Zynq US+ MPSoC (11/17/19-EG) SOM

Processor: Xilinx's Zynq US+ MPSoC (11/17/19-EG)

RAM: 4GB PS DDR4*
4GB Dual PL DDR4*

Application: Video Surveillance, Cloud Computing, Artificial Intelligence/Machine Learning, 5G Wireless, High Precision Test Instrument.

** RAM size is expandable. Contact iWave team for further details*

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Headquarters: INDIA

iWave Systems Tech. Pvt. Ltd.

7/B, 29th Main, BTM Layout 2nd Stage,
Bengaluru-560076, India.

Ph: +91-80-26683700, 26781643

Email: mktg@iwavesystems.com

www.iwavesystems.com

JAPAN

iWave Japan, Inc.

8F-B, Kannai Sumiyoshi Building,
3-29, Sumiyoshi-cho, Naka-ku, Yokohama,
Kanagawa, Japan.

Email: mktg@iwavesystems.com

UNITED STATES

iWave USA

1692 Westmont Ave., Campbell,
CA95008 USA

Ph: 408-206-5958

Email: info@iwavesystems.us

EUROPE

iWave Europe.

International Sales and Marketing,
Europe.

Venkelbaan 55 2908KE Capelle
aan den IJssel

Email: info@iwavesystems.eu

Our Partners Across The Globe

GLOBAL

Arrow Electronics, Inc.

9201 East Dry Creek Road
Centennial, CO 80112 USA
NA: +1-855-326-4757
websupport@arrow.com
EMEA: +49 (0) 6102 5030 0
esc@arroweurope.com
Asia: +86 0755 82505643
peter.hong@arrowasia.com

ONLINE

Digi-Key Corporation

701 Brooks Avenue South
Thief River Falls,
MN 56701-0677
Tel: +1 800-344-4539
Fax: +1 218-681-3380
E-mail: sales@digikey.com

USA

Embedded Technologies, Inc

2870 Scott St, Suite 101,
Vista, California, USA,
Tel: +1 760 5982870,
E-mail: info@embeddedtechnologies.com

TURKEY

ÖZDİSAN ELEKTRONİK A.Ş.

DES Sanayi Sitesi 104 Sokak A07,
54-56 Upper Dudullu / Ümraniye,
İstanbul - Turkey
Tel: +90 216 420 18 82
Fax: +90 216 466 36 82
E-mail: info@ozdisan.com

GLOBAL

Future Electronics

237 Hymus Blvd.,
Pointe Claire, Quebec,
Canada H9R 5C7.
Tel: 514-694-7710
Email: eservices@futureelectronics.com
EMEA: +44 178 427 5000
FES-EMEA@FutureElectronics.com
Asia: info-sales-asia@futureelectronics.com

BENELUX

Batenburg Applied Technologies

Stolwijkstraat 33, 3079 DN
Rotterdam.
Tel: +31 (0)10 2580580,
+32 (0)474 229609
Email: marcel.koot@batenburg.nl, be

POLAND

ME Embedded Sp. z o.o.

Staniewicka 14 street,
03-310 Warsaw, Poland.
Tel: +48 797 383 766
Email: info@me-embedded.eu

SWEDEN

Acte Solutions AB

Box 4115,
SE-171 04 Solna,
Sweden.
Tel: +46 8 445 2800 / 46
Email: henrik.svedlund@acte.se

GLOBAL

Mouser Electronics, Inc.

1000 North Main Street
Mansfield, Texas 76063
Tel: +1 800-346-6873
Fax: +1 817-804-3899
E-mail: sales@mouser.com

FRANCE

EUROCOMPOSANT

1, rue René Caudron - BP 15
78960 Voisins-le-Bretonneux,
France
Tel: +33-130649515
Fax: +33-130436827
Email: contact@eurocomposant.fr

KOREA

J.S Communications

913, Dojung Tower, Anyang-ro 115,
Manan-gu, Anyang-si, Gyeonggi-do, Korea
Tel : +82-31-349-9793
Email: scott.lee@jscoms.co.kr

SPAIN

Anatronic

Paseo de los Melancólicos, N° 9-2° A
28005 MADRID, Spain
Tel : +34 91 366 01 59
Email: bpater@anatronic.com