iW-RainboW-G40M
i.MX 8M Plus Quad/QuadLite/Dual
SMARC System On Module
Hardware User Guide

iWave
Embedding Intelligence

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the SMARC V2.1.1 SOM based on the NXP's i.MX 8M Plus (Quad/QuadLite/Dual) Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8M Plus SMARC SOM from a Hardware Systems perspective.

1.2 SMARC SOM Overview

The SMARC V2.1.1 ("Smart Mobility ARChitecture version 2.1.1") is a versatile small form factor Computer Module definition targeting application that require low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies, GbE, GNSS module (optional) and dual channel LVDS/ MIPI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8M Plus SoC based SMARC System on Module is rich with i.MX 8M Plus features along with on SOM LPDDR4, eMMC, Dual Ethernet PHY (one with TSN support), USB2.0 Hub, Wi-Fi & BT module, GNSS module (optional) and comes in compact 82mm x 50mm form factor. The Module PCB has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DP	Display Port
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
EMS	Electronics manufacturing services
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SMARC	Smart Mobility ARChitecture
SoC	System on Chip
SOM	System On Module
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
HCSL	High speed Current Steering Logic
LVDS	Low Voltage Differential Signal
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
SATA	Serial Advanced Technology Attachment differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- IMX8MPXEC_Rev_x.pdf
- iMX_8M_Plus_RM_Revx.pdf
- SMARC Specification v2.1.1

1.6 Important Note

In this document, wherever i.MX 8M Plus SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "F*unctionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8M Plus SMARC SOM features and Hardware architecture with high level block diagram.

2.1 i.MX 8M Plus SMARC SOM Block Diagram

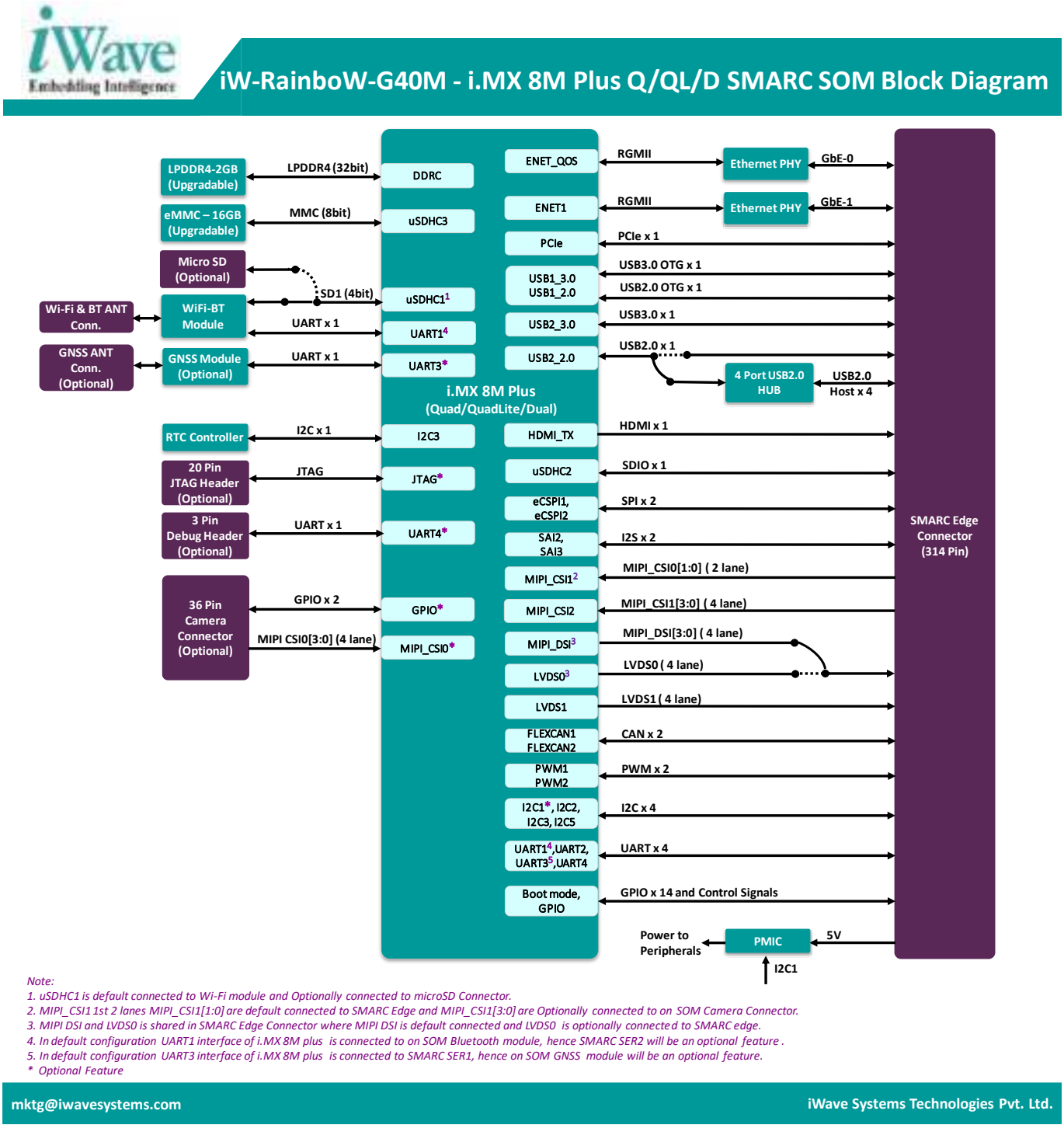


Figure 1: i.MX 8M Plus SMARC SOM Block Diagram

2.2 i.MX 8M Plus SMARC SOM Features

i.MX 8M Plus SMARC SOM supports the following features.

SoC

- i.MX 8M Plus Applications Processor[1]:
  - i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi 4 Audio DSP
  - i.MX 8M Plus QuadLite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
  - i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi 4 Audio DSP

Power

- PCA9450C PMIC

Memory

- LPDDR4 - 2GB (Expandable up to 8GB)[1]
- eMMC Flash - 16GB (Expandable up to 128GB)[1]
- Micro SD Connector (Optional)[3]

Other On-SOM Features

- Wi-Fi 802.11a/b/g/n/ac + BT 5.0 Module[2]
- Gigabit Ethernet PHY Transceiver x 2
- USB 2.0 High Speed 4-Port Hub
- RTC Controller
- FAN Header
- GNSS Module (Optional)[3]
- Debug UART Header (Optional)
- JTAG Header (Optional)

MIPI-CSI Camera Connector (Optional)

- MIPI CSI x 1 Channel (1 x 4lane)
- I2C x 1 Port

SMARC PCB Edge Interfaces

- Gigabit Ethernet x 2 Ports (through On-SOM Gigabit Ethernet PHY transceiver)
- SD (4bit) x 1 Port
- USB 3.0 OTG x 1 Port (Including USB2.0 lanes)
- USB3.0 Host x 1 Port
- USB 2.0 Host x 4Ports (through On-SOM USB Hub)
- PCIe x 1 Ports
- MIPI CSI x 2 Channel (1 x 2 Lane and 1 x 4 Lane)
- HDMI 2.0 Transmitter x 1 Port

- LVDS0/MIPI DSI x 1 Channel[4] (1 x 4Lane)
- LVDS1 x 1 Channel (1 x 4Lane)
- SAI/I2S (Audio Interface) x 2 Port
- SPI x 2 Port
- Data UART (with CTS & RTS) x 1 Port[5]
- Data UART (without CTS & RTS) x 2 Port (One port can be used as Debug Port)[3]
- SMARC GPIO x 14[6]
- CAN FD x 2 Port
- I2C x 4 Ports
- PWM x 2

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 82mm X 50mm (SMARC V2.1.1 Specification)

1. *Memory Size will differ based on iWave's SOM Product Part Number.*
2. *In Murata-1MW, Wi-Fi is supported by using SDIO interface, hence On SOM microSD will be an optional feature.*
3. *In default configuration, UART3 interface of i.MX 8M Plus is connected to SMARC Edge. If on SOM GNSS module is used, UART3 will not be supported on SMARC Edge.*
4. *The i.MX 8M Plus supports MIPI_DSI and LVDS interface, but in SMARC Specification LVDS and MIPI_DSI interface pins are multiplexed hence any one can be supported at a time based on SOM part Number. By default, MIPI DSI is supported.*
5. *In default configuration, UART1 interface of i.MX 8M Plus is connected to on SOM Bluetooth module. One more UART with CTS and RTS can be supported, if Bluetooth is not supported.*
6. *In default configuration, SMARC GPIOs 12 and 14 are not supported and instead LVDS1 VDD_Enable and Backlight Enable GPIOs are supported.*

2.3 i.MX 8M Plus SoC

iW-RainboW-G40M SMARC SOM can support i.MX 8M Plus SoCs from NXP. The i.MX 8M Plus Family consists of three processors: i.MX 8M Plus Quad, i.MX 8M Plus QuadLite & i.MX 8M Plus Dual. The Major Difference between i.MX 8M Plus SoCs are:

- i.MX 8M Plus Quad : 4 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi 4 Audio DSP
- i.MX 8M Plus QuadLite : 4 x Cortex-A53, 1 x Cortex-M7 & GPU
- i.MX 8M Plus Dual : 2 x Cortex-A53, 1 x Cortex-M7, GPU, VPU, NPU, ISP & HiFi 4 Audio DSP

The i.MX 8M Plus processors along with ARM core supports integrated NPU of 2.3 TOPs, OpenCL GPU, Image Signal Processor, 1080p60 video encode and decode capable VPU, 3 x display controllers, multiple display output options, including MIPI-DSI, HDMI 2.0, and LVDS. Memory interfaces supporting LPDDR4, FlexSPI, eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

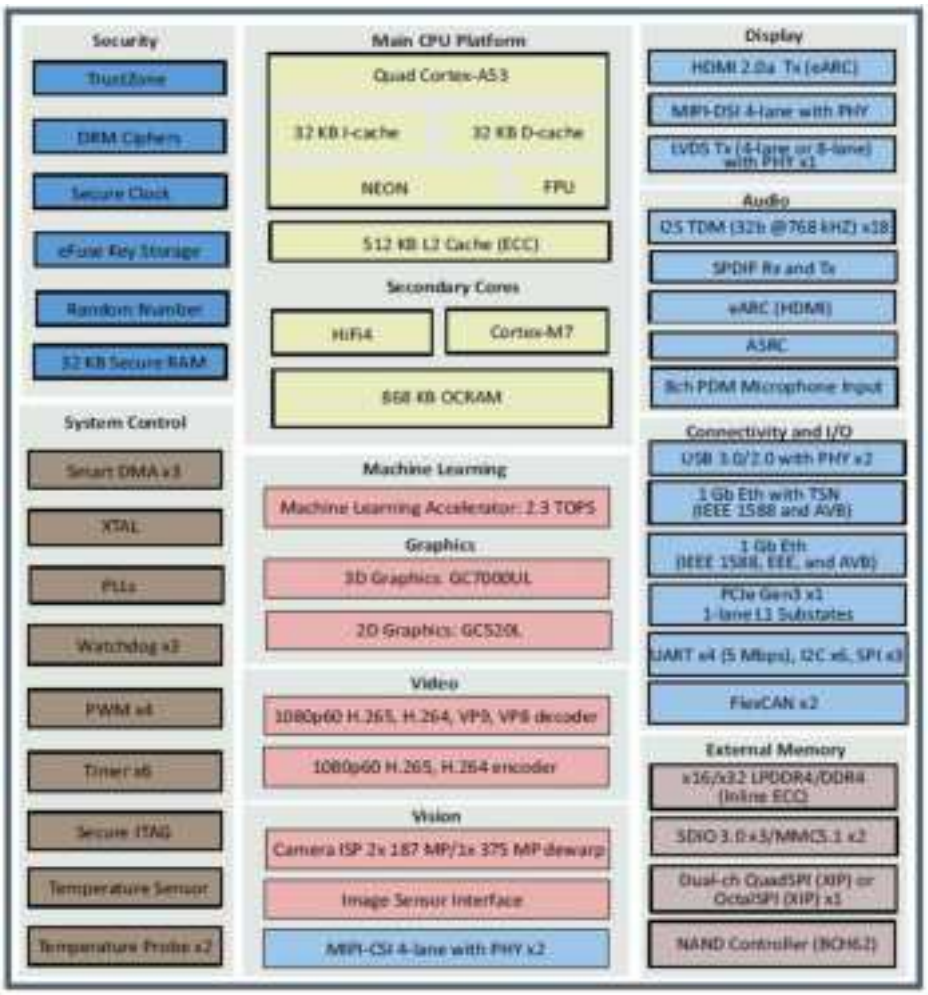


Figure 2: i.MX 8M Plus Block Diagram

Note: The i.MX 8M Plus processor offers numerous advanced features, please refer the latest i.MX 8M Plus Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PCA9450C PMIC

The i.MX 8M Plus SMARC SOM uses one PCA9450C PMIC (U9) for SOM Power management. The PCA9450C features six high efficiency step-down regulators and five linear regulators. It is a high-performance power management integrated circuit (PMIC) that provides a highly programmable/configurable architecture with fully integrated power devices and built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9450C PMIC comes in 56pin 7x7 HVQFN Package and is placed on the Top side of the SOM.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8M Plus SMARC SOM supports 2GB LPDDR4 RAM memory by default using the 32bit DDR_CH0 channel of i.MX 8M Plus SoC to support LPDDR4 up to 2GHz speed. LPDDR4 part U14 is placed on Top side of the SOM. The RAM size can be expandable up to maximum of 8GB. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 8M Plus SMARC SOM supports 16GB eMMC as default boot and storage device. This is directly connected to uSDHC3 controller of the i.MX 8M Plus SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash memory (U30) is physically located on bottom side of the SMARC SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector (Optional)

The i.MX 8M Plus SMARC SOM optionally supports Micro SD connector which can be used to connect Micro SD card as optional Mass storage device. Micro SD card connector (J5) is connected to the USDHC1 controller of the i.MX 8M Plus SoC.

The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8M Plus SMARC SOM supports configurable I/O voltage levels for USDHC1 lines through GPIO1_IO03. If GPIO1_IO03 is set to low, then 3.3V IO level is selected for uSDHC1 lines. If GPIO1_IO03 is set to high, then 1.8V IO level is selected for uSDHC1 lines. Micro SD Connector is physically located on Top side of the i.MX 8M Plus SMARC SOM.

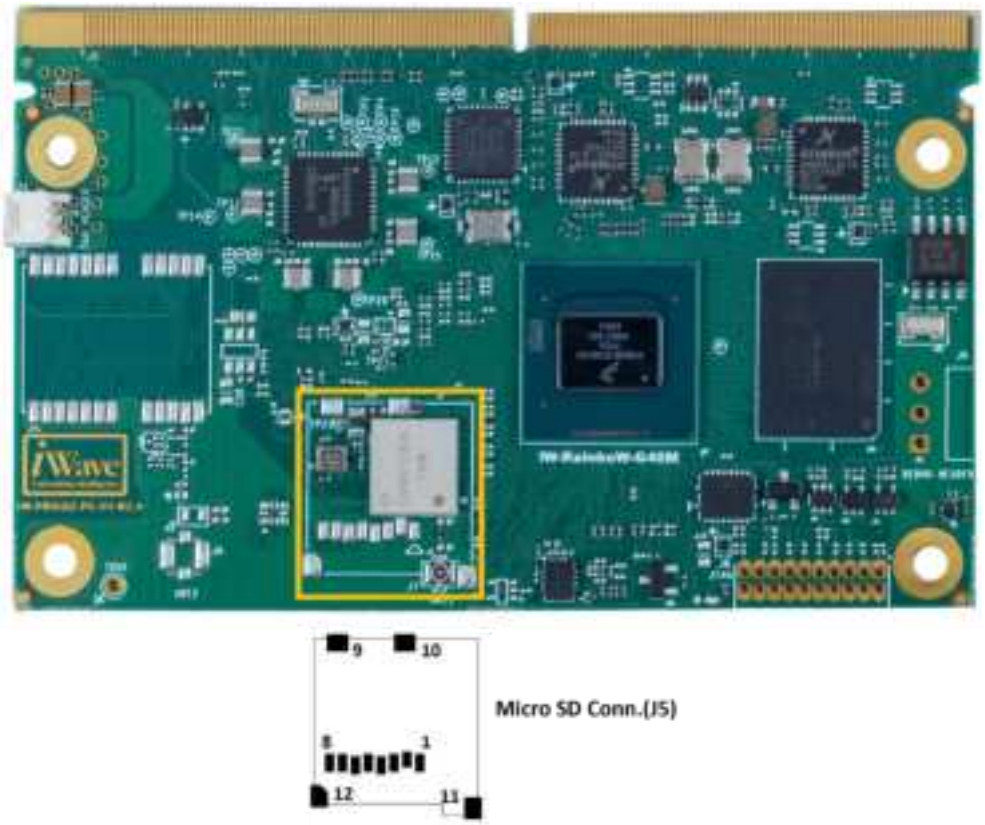


Figure 3: Micro SD Connector

Note: In default configuration USDHC1 is used for on board Wi-Fi module. Contact iWave Support team if microSD feature is required or refer Application Note: "AN4004-i.MX 8M PLUS SMARC SOM-Enabling On SOM Micro SD Support-Application Note-R2.0-REL1.1.pdf"

2.6 Network & Communiation

2.6.1 Wi-Fi and Bluetooth Interface

The i.MX 8M Plus SMARC SOM is integrated with Murata's "LBEE5HY1MW" based Wi-Fi & Bluetooth module. The LBEE5HY1MW module is a very high-performance module based on Cypress CYW43455 combo chipset which supports WiFi IEEE 802.11a/b/g/n/ac + Bluetooth 5.0 BDR/EDR/LE standard.

The LBEE5HY1MW module utilizes highly optimized IEEE 802.11 Bluetooth coexistence protocols and supports single stream 1x1 IEEE 802.11 a/b/g/n/ac mode providing up to 390Mbps. The LBEE5HY1MW module features small form factor when integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive switch, Power Management. The LBEE5HY1MW module need external Antenna and a 32.768 KHz clock for sleep operation.

The LBEE5HY1MW module (U19) provides Secure Digital Input Output (SDIO) for interfacing with the host controller for Wi-Fi and UART interface for Bluetooth. The i.MX 8M Plus SMARC SOM uses processor's UART1 interface for

Bluetooth and USDHC1 interface for Wi-Fi in default configuration. In i.MX 8M Plus SMARC SOM, antenna pin of Wi-Fi & Bluetooth module is connected to J7 Connector.

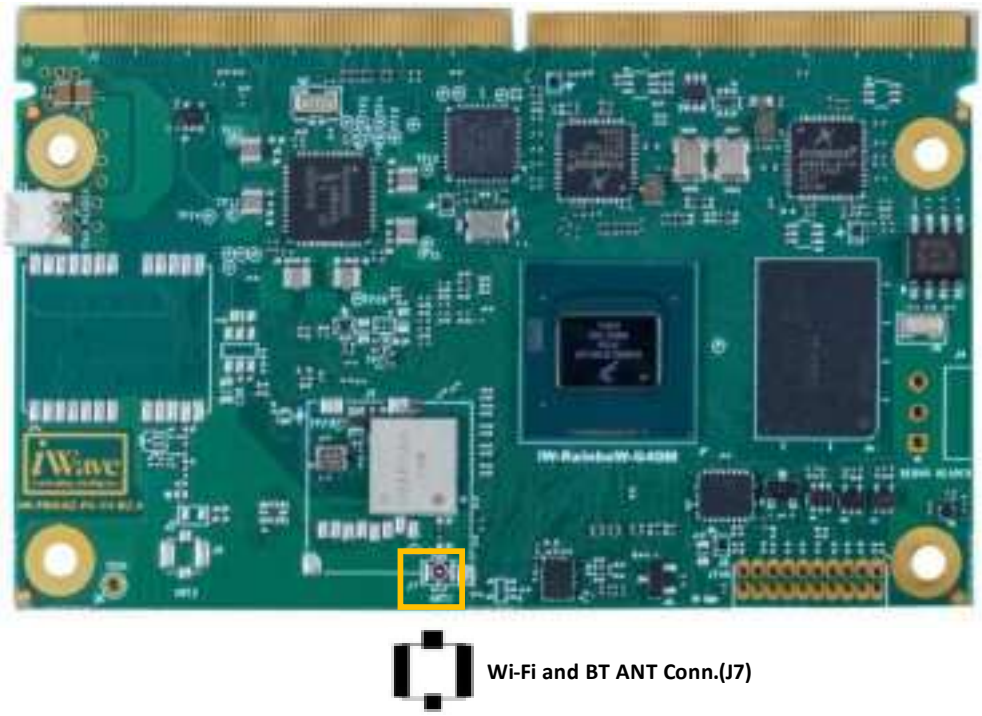


Figure 4: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata Electronics.

Antenna Part Number - : 2042811100 from Molex

Note: The operating temperature range of LBEE5HY1MW module is -30°C to 85°C .

2.6.2 GNSS Module (Optional)

The i.MX 8M Plus SMARC SOM can be optionally integrated with u-blox's "NEO-M8Q-01A" based GNSS module. The NEO-M8Q-01A module is built on the exceptional performance of the u-blox M8 GNSS engine in the industry proven NEO form factor. It utilizes concurrent reception of up to three GNSS systems (GPS/Galileo together with BeiDou or GLONASS) for more reliable positioning.

The NEO-M8Q-01A provides high sensitivity and minimal acquisition times while maintaining low system power. The NEO-M8Q-01A combines a high level of robustness and integration capability along with flexible connectivity options via USB, I2C, UART and SPI. The DDC (I2C compatible) interface provides connectivity and enables synergies with most u-blox cellular modules.

The i.MX 8M Plus SMARC SOM makes use of the UART3 interface which is by default connected to the SMARC Edge connector for communication between the Host and Device. The Antenna pin of the module can be connected to the J6 Antenna connector through an Active or Passive Path as per the requirement.

Connector Part Number - : 734120110 from Molex.

Antenna Part Number - : TBD

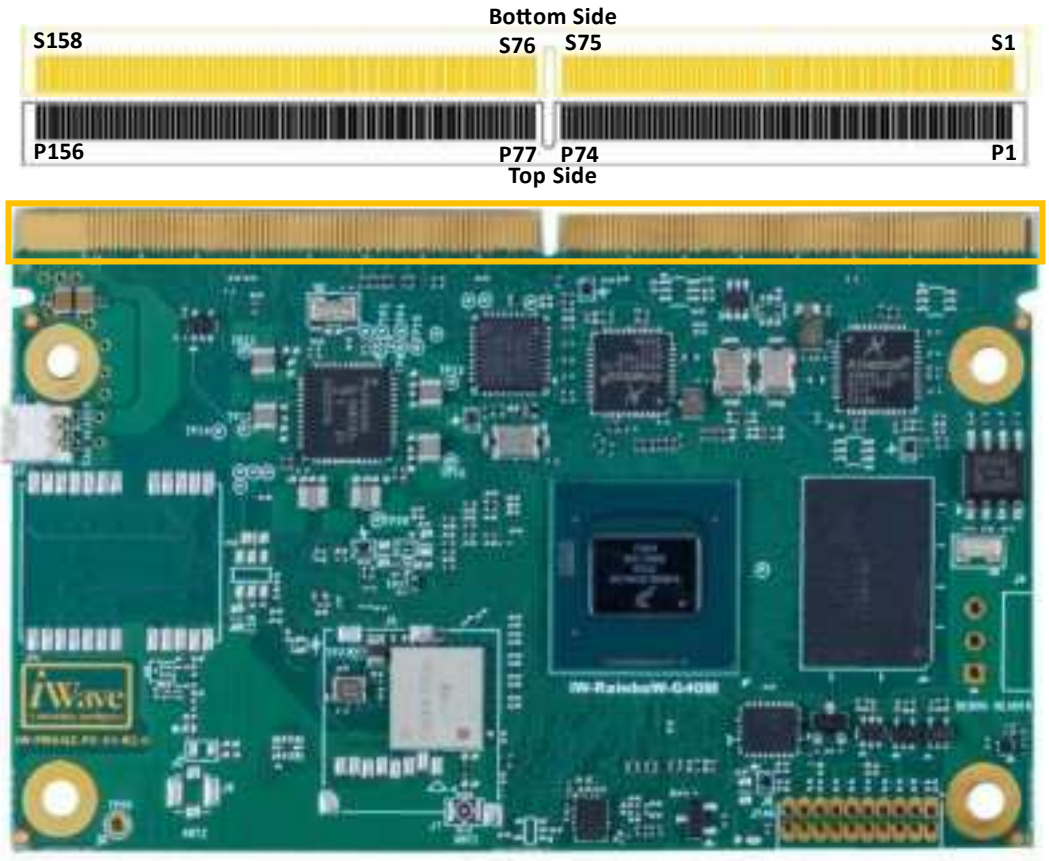
Note: In default configuration GNSS Module is not populated. Contact iWave Support team if GNSS feature is required or refer Application Note: "AN4005-i.MX 8M PLUS SMARC SOM-Enabling On SOM GNSS Support-Application Note-R2.0-REL1.0.pdf"

2.6.3 RTC Controller

The i.MX 8M Plus SMARC SOM uses the On-SOM external RTC Controller "PCF85263" for Real time clock support. This external RTC Controller is connected to i.MX 8M Plus SoC through I2C3 Interface and operates at 1.8V voltage level. In SOM power off condition, this device will take 3V power from SMARC PCB Edge (VDD_RTC) coin cell power input (Pin S147) and continues to update the current time. GPIO4_20 is connected to the Interrupt pin of the RTC controller, which can be utilized for supporting wakeup and other features.

2.7 SMARC PCB Edge Connector

SMARC PCB edge connector (J1) has standard pinout as per SMARC Specification V2.1.1. The interfaces which are available at 314pin SMARC Edge connector are explained in the following sections.



SMARC PCB Edge Connector(J1)

Figure 5: SMARC Edge Connector

Number of Pins - : 314

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 91782-3140M-001 from Aces

Table 3: SMARC Edge Connector Pinouts

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
GPIO_SMB_ALERT_GPIO5_02	**P1**	**S1**	I2C5_SCL(SPDIF_TX)
GND	**P2**	**S2**	I2C5_SDA(SPDIF_RX)
MIPI_CSI2_CLK_P	**P3**	**S3**	GND
MIPI_CSI2_CLK_N	**P4**	**S4**	NC
GBE1_PPS_SDP	**P5**	**S5**	I2C3_SCL
GBE0_PPS_SDP	**P6**	**S6**	CAMERA_CCMCLKO1(ECSPI2_MISO)
MIPI_CSI2_D0_P	**P7**	**S7**	I2C3_SDA
MIPI_CSI2_D0_N	**P8**	**S8**	MIPI_CSI1_CLK_P
GND	**P9**	**S9**	MIPI_CSI1_CLK_N
MIPI_CSI2_D1_P	**P10**	**S10**	GND
MIPI_CSI2_D1_N	**P11**	**S11**	MIPI_CSI1_D0_P
GND	**P12**	**S12**	MIPI_CSI1_D0_N
MIPI_CSI2_D2_P	**P13**	**S13**	GND
MIPI_CSI2_D2_N	**P14**	**S14**	MIPI_CSI1_D1_P
GND	**P15**	**S15**	MIPI_CSI1_D1_N
MIPI_CSI2_D3_P	**P16**	**S16**	GND
MIPI_CSI2_D3_N	**P17**	**S17**	GBE1_MDI0+
GND	**P18**	**S18**	GBE1_MDI0-
GBE0_MDI3-	**P19**	**S19**	GBE1_LINK100#
GBE0_MDI3+	**P20**	**S20**	GBE1_MDI1+
GBE0_LINK100#	**P21**	**S21**	GBE1_MDI1-
GBE0_LINK1000#	**P22**	**S22**	GBE1_LINK1000#
GBE0_MDI2-	**P23**	**S23**	GBE1_MDI2+
GBE0_MDI2+	**P24**	**S24**	GBE1_MDI2-
GBE0_LINK_ACT#	**P25**	**S25**	GND
GBE0_MDI1-	**P26**	**S26**	GBE1_MDI3+
GBE0_MDI1+	**P27**	**S27**	GBE1_MDI3-
VPHY0_DVDDL	**P28**	**S28**	VPHY1_DVDDL
GBE0_MDI0-	**P29**	**S29**	NC (Optionally GBE0_SOP)
GBE0_MDI0+	**P30**	**S30**	NC (Optionally GBE0_SON)
NC	**P31**	**S31**	GBE1_LINK_ACT#
GND	**P32**	**S32**	NC (Optionally GBE0_SIP)
GPIO2_20(SD2_WP)	**P33**	**S33**	NC (Optionally GBE0_SIN)
SD2_CMD	**P34**	**S34**	GND
GPIO2_12(SD2_CD_B)	**P35**	**S35**	USB_HUB3OUT_DP
SD2_CLK	**P36**	**S36**	USB_HUB3OUT_DM
GPIO2_19(SD2_RESET_B)	**P37**	**S37**	VBUS_OTG1
GND	**P38**	**S38**	SAI2_MCLK
SD2_DATA0	**P39**	**S39**	SAI2_TX_SYNC(SAI2_TXFS)

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
SD2_DATA1	**P40**	**S40**	SAI2_TX_DATA0(SAI2_TXD0)
SD2_DATA2	**P41**	**S41**	SAI2_RX_DATA0(SAI2_RXD0)
SD2_DATA3	**P42**	**S42**	SAI2_TX_BCLK(SAI2_TXC)
ECSPI1_SS0	**P43**	**S43**	NC
ECSPI1_SCLK	**P44**	**S44**	NC
ECSPI1_MISO	**P45**	**S45**	NC (Optionally SMARC_MDIO_CLK)
ECSPI1_MOSI	**P46**	**S46**	NC (Optionally SMARC_MDIO_DATA)
GND	**P47**	**S47**	GND
NC	**P48**	**S48**	I2C2_SCL
NC	**P49**	**S49**	I2C2_SDA
GND	**P50**	**S50**	SAI3_TX_SYNC(SAI3_TXFS)
NC	**P51**	**S51**	SAI3_TX_DATA0(SAI3_TXD)
NC	**P52**	**S52**	SAI3_RX_DATA0(NAND_DATA00)
GND	**P53**	**S53**	SAI3_TX_BCLK(SAI3_TXC)
ECSPI2_SS0	**P54**	**S54**	NC
NC	**P55**	**S55**	USB_HUB4_OC
ECSPI2_SCLK	**P56**	**S56**	NC
ECSPI2_MISO(I2C4_SCL)	**P57**	**S57**	NC
ECSPI2_MOSI	**P58**	**S58**	NC
GND	**P59**	**S59**	USB_HUB4OUT_DP
NC (Optionally USB_OTG1_DP)	**P60**	**S60**	USB_HUB4OUT_DM
NC (Optionally USB_OTG1_DM)	**P61**	**S61**	GND
NC (Optionally USB1_OTG_OC(GPIO1_IO13))	**P62**	**S62**	USB1_TX_P
NC (Optionally VBUS_OTG1)	**P63**	**S63**	USB1_TX_N
NC (Optionally USB_OTG1_ID)	**P64**	**S64**	GND
USB_HUB1OUT_DP	**P65**	**S65**	USB1_RX_P
USB_HUB1OUT_DM	**P66**	**S66**	USB1_RX_N
USB_HUB1_OC	**P67**	**S67**	GND
GND	**P68**	**S68**	USB_OTG1_DP
USB_HUB2OUT_DP	**P69**	**S69**	USB_OTG1_DM
USB_HUB2OUT_DM	**P70**	**S70**	GND
USB_HUB2_OC	**P71**	**S71**	USB2_TX_P
NC	**P72**	**S72**	USB2_TX_N
NC	**P73**	**S73**	GND

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
USB1_OTG_OC(GPIO1_IO13)	**P74**	**S74**	USB2_RX_P
		S75	USB2_RX_N
Key			
GPIO_PCIE_RST(GPIO1_IO12)	**P75**	**S76**	NC
USB_HUB3_OC	**P76**	**S77**	NC
NC	**P77**	**S78**	NC (Optionally GBE1_SIP)
NC (Optional PCIE_CLKREQ_B(SAI3_MCLK))	**P78**	**S79**	NC (Optionally GBE1_SIN)
GND	**P79**	**S80**	GND
NC	**P80**	**S81**	NC (Optionally GBE1_SOP)
NC	**P81**	**S82**	NC (Optionally GBE1_SON)
GND	**P82**	**S83**	GND
PCIE_REFCLK_DP	**P83**	**S84**	NC
PCIE_REFCLK_DM	**P84**	**S85**	NC
GND	**P85**	**S86**	GND
PCIE_RXN_P	**P86**	**S87**	NC
PCIE_RXN_N	**P87**	**S88**	NC
GND	**P88**	**S89**	GND
PCIE_TXN_P	**P89**	**S90**	NC
PCIE_TXN_N	**P90**	**S91**	NC
GND	**P91**	**S92**	GND
HDMI_TX_D2_P	**P92**	**S93**	NC
HDMI_TX_D2_N	**P93**	**S94**	NC
GND	**P94**	**S95**	NC
HDMI_TX_D1_P	**P95**	**S96**	NC
HDMI_TX_D1_N	**P96**	**S97**	NC
GND	**P97**	**S98**	NC
HDMI_TX_D0_P	**P98**	**S99**	NC
HDMI_TX_D0_N	**P99**	**S100**	NC
GND	**P100**	**S101**	GND
HDMI_TX_CLK_P	**P101**	**S102**	NC
HDMI_TX_CLK_N	**P102**	**S103**	NC
GND	**P103**	**S104**	USB_OTG1_ID
HDMI_TX_HPD	**P104**	**S105**	NC
HDMI_TX_DDC_SCL	**P105**	**S106**	NC
HDMI_TX_DDC_SDA	**P106**	**S107**	SMARC_GPIO_12_GPIO3_21(NAND_DQS)
NC (Optionally GPIO3_IO28(HDMI_CEC))	**P107**	**S108**	LVDS1_CLK_P
SMARC_GPIO_0_GPIO4_18(SAI1_TXD6)	**P108**	**S109**	LVDS1_CLK_N
SMARC_GPIO_1_GPIO4_19(SAI1_TXD7)	**P109**	**S110**	GND

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
SMARC_GPIO_2_GPIO4_0(SAI1_RXFS)	**P110**	**S111**	LVDS1_D0_P
SMARC_GPIO_3_GPIO4_1(SAI1_RXC)	**P111**	**S112**	LVDS1_D0_N
SMARC_GPIO_4_GPIO4_2(SAI1_RXD0)	**P112**	**S113**	NC
SMARC_GPIO_5_GPIO3_20(SAI5_RXC)	**P113**	**S114**	LVDS1_D1_P
SMARC_GPIO_6_GPIO4_22(SAI2_RXC)	**P114**	**S115**	LVDS1_D1_N
SMARC_GPIO_7_GPIO4_21(SAI2_RXFS)	**P115**	**S116**	SMARC_GPIO_13_GPIO3_28(HDMI_CEC)
SMARC_GPIO_8_GPIO4_28(SAI3_RXFS)	**P116**	**S117**	LVDS1_D2_P
SMARC_GPIO_9_GPIO4_3(SAI1_RXD1)	**P117**	**S118**	LVDS1_D2_N
SMARC_GPIO_10_GPIO3_21(SAI5_RXFS)	**P118**	**S119**	GND
SMARC_GPIO_11_GPIO5_5(SPDIF1_EXT_CLK)	**P119**	**S120**	LVDS1_D3_P
GND	**P120**	**S121**	LVDS1_D3_N
NC (Optionally I2C1_SCL)	**P121**	**S122**	PWM2_OUT(SAI5_RXD0)
NC (Optionally I2C1_SDA)	**P122**	**S123**	NC (Optionally SMARC_GPIO_13_GPIO3_28(HDMI_CEC))
BOOT_SEL0#	**P123**	**S124**	GND
BOOT_SEL1#	**P124**	**S125**	LVDS0/DSI0_D0_P
BOOT_SEL2#	**P125**	**S126**	LVDS0/DSI0_D0_N
GPIO_RESET_OUT_GPIO1_9_1V8	**P126**	**S127**	LCD0_BKLT_EN_GPIO3_7(NAND_DATA01)
PMIC_RST_B	**P127**	**S128**	LVDS0/DSI0_D1_P
CPU_ON_OFF	**P128**	**S129**	LVDS0/DSI0_D1_N
UART2_TXD	**P129**	**S130**	GND
UART2_RXD	**P130**	**S131**	LVDS0/DSI0_D2_P
UART2_CTS_B(SAI3_RXC)	**P131**	**S132**	LVDS0/DSI0_D2_N
UART2_RTS_B(SAI3_RXD)	**P132**	**S133**	LCD0_VDD_EN_GPIO3_8(NAND_DATA02)
GND	**P133**	**S134**	LVDS0/DSI0_CLK_P
UART3_TXD	**P134**	**S135**	LVDS0/DSI0_CLK_N
UART3_RXD	**P135**	**S136**	GND
NC (Optionally UART1_TX)	**P136**	**S137**	LVDS0/DSI0_D3_P
NC (Optionally UART1_RX)	**P137**	**S138**	LVDS0/DSI0_D3_N
NC (Optionally UART1_CTS_B)	**P138**	**S139**	I2C5_SCL(SPDIF_TX)
NC (Optionally UART1_RTS_B)	**P139**	**S140**	I2C5_SDA(SPDIF_RX)
UART4_TXD	**P140**	**S141**	PWM1_OUT(I2C4_SDA)
UART4_RXD	**P141**	**S142**	NC (Optionally SMARC_GPIO_12_GPIO3_21(NAND_DQS))
GND	**P142**	**S143**	GND
FLEXCAN1_TX(SAI5_RXD1)	**P143**	**S144**	NC

Signal	SMARC Pins (Top)	SMARC Pins (Bottom)	Signal
FLEXCAN1_RX(SAI5_RXD2)	**P144**	**S145**	GPIO_WDT_OUT
FLEXCAN2_TX(SAI5_RXD3)	**P145**	**S146**	GPIO_PCIe_Wake(GPIO1_IO14)
FLEXCAN2_RX(SAI5_MCLK)	**P146**	**S147**	VRTC_3V0
VDD_IN	**P147**	**S148**	NC
VDD_IN	**P148**	**S149**	NC
VDD_IN	**P149**	**S150**	VIN_PWR_BAD#
VDD_IN	**P150**	**S151**	NC
VDD_IN	**P151**	**S152**	NC
VDD_IN	**P152**	**S153**	CARRIER_STBY#
VDD_IN	**P153**	**S154**	CARRIER_PWR_ON
VDD_IN	**P154**	**S155**	FORCE_RECOV#
VDD_IN	**P155**	**S156**	NC
VDD_IN	**P156**	**S157**	TEST#
		S158	GND

2.7.1 Gigabit Ethernet

The i.MX 8M Plus SMARC SOM supports two Gigabit Ethernet using the two on SOM Ethernet PHY "AR8031" from Atheros, Qualcomm. ENET0 and ENET1 of i.MX 8M Plus SoC are connected to GBE0 and GBE1 ports of SMARC edge connector respectively. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements. The GBE0 of i.MX 8M Plus SMARC SOM also optionally supports TSN feature. Contact iWave if TSN support is required.

For more details on GBE0 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P6	GBE0_SDP	GBE0_PPS_SDP	NA	IO, 3.3V CMOS	NC. *Note: Optionally connected to GBE0_PPS_SDP*
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	O, 3.3V CMOS 10K PU	100Mbps Ethernet link status LED. *Note: Connect to Cathode of LED.*
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	O, 3.3V CMOS 10K PU	Gigabit Ethernet link status LED. *Note: Connect to Cathode of LED.*
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	O, 3.3V CMOS 10K PU	Gigabit Ethernet activity status *Note: Connect to Cathode of LED.*
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of the magnetics.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.

For more details on GBE1 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P5	GBE1_SDP	GBE1_PPS_SDP	NA	IO, 3.3V CMOS	NC. *Note: Optionally connected to GBE1_PPS_SDP*
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	O, 3.3V CMOS 10K PU	100Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	O, 3.3V CMOS 10K PU	1000Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair2 negative.
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	GBE1_CTREF	VPHY1_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	O, 3.3V CMOS	Ethernet Activity status LED.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				10K PU	*Note: Connect to Cathode of LED.*

2.7.2 MDIO Interface (Optional)

The i.MX 8M Plus SMARC SOM optionally supports MDIO support from the ENET MDIO of the i.MX 8M Plus processor on the SMARC Edge connector.

For more details on MDIO pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S45	MDIO_CLK	SMARC_MDIO_CLK	NA	O, 1.8V CMOS	NC. *Note: Optionally connected to ENET1_MDC*
S46	MDIO_DAT	SMARC_MDIO_DATA	NA	IO, 1.8V CMOS	NC. *Note: Optionally connected to ENET1_MDIO*

2.7.3 SD Interface

The i.MX 8M Plus SMARC SOM supports 4bit SD interface over SMARC PCB Edge connector which can be used to connect SD card as Mass storage or boot device. uSDHC2 controller of the i.MX 8M Plus SoC is used to support SMARC SD interface. uSDHC2 operates both in 3.3V and 1.8V IO level and supports maximum card bus frequency of 208 MHz. The i.MX 8M Plus SMARC SOM supports configurable I/O voltage levels for USDHC2 lines through GPIO1_IO4. If GPIO1_IO4 is set to low, then 3.3V IO level is selected for uSDHC2 lines. If GPIO1_IO4 is set to high, then 1.8V IO level is selected for uSDHC2 lines. Control GPIOs like Write Protect and Card detect signals also operates at both 1.8V and 3.3V IO level.

For more details on SD pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P33	SDIO_WP	GPIO2_20(SD2_WP)	SD2_WP/ AC26	I, 1.8/3.3V CMOS 10K PU	SD write Protect.
P34	SDIO_CMD	SD2_CMD	SD2_CMD/ AB28	IO, 1.8/3.3V CMOS	SD command. *Note: 10K pullup option is provided.*
P35	SDIO_CD#	GPIO2_12(SD2_CD_B)	SD2_CD_B/ AD29	I, 1.8V/3.3V CMOS 10K PU	SD Card Detect.
P36	SDIO_CK	SD2_CLK	SD2_CLK/	O, 1.8/3.3V	SD Clock

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
			AB29	CMOS	*Note: 1K pullup option is provided.*
P37	SDIO_PWR_EN	GPIO2_19(SD2_RESET_B)	SD2_RESET_B / AD28	O, 3.3V CMOS	SD Power enable.
P39	SDIO_D0	SD2_DATA0	SD2_DATA0/ AC28	IO, 1.8/3.3V CMOS	SD data 0 *Note: 10K pullup option is provided.*
P40	SDIO_D1	SD2_DATA1	SD2_DATA1/ AC29	IO, 1.8/3.3V CMOS	SD data 1. *Note: 10K pullup option is provided*
P41	SDIO_D2	SD2_DATA2	SD2_DATA2/ AA26	IO, 1.8/3.3V CMOS	SD data 2. *Note: 10K pullup option is provided*
P42	SDIO_D3	SD2_DATA3	SD2_DATA3/ AA25	IO, 1.8/3.3V CMOS	SD data 3. *Note: 10K pullup option is provided*

2.7.4 USB3.0 OTG Interface

The i.MX 8M Plus SMARC SOM supports one USB 3.0 OTG interface and one USB3.0 Host port on SMARC PCB Edge connector. Also, it supports four USB2.0 Host interface on SMARC PCB Edge connector through On-SOM USB 2.0 four port hub.

i.MX 8M Plus SoC's USB OTG1 controller with integrated PHY used for USB 3.0 OTG interface is directly connected to USB3 port of SMARC PCB Edge connector. This USB3.0 OTG is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports USB dual-role operation and can be configured as host or device. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

For more details on USB pinouts near SMARC edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S37	USB3_VBUS_DET	VBUS_OTG1	NA	I, Power	USB 3.0 OTG VBUS power for detection. *Note: Same power is also connected to P63rd pin through resistor and default not populated.*
S62	USB3_SSTX+	USB1_TX_P	USB1_TX_P/ A10	O, USB SS/ 0.1uf AC coupled	USB 3.0 OTG Super Speed Transmit Positive.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S63	USB3_SSTX-	USB1_TX_N	USB1_TX_N/ B10	O, USB SS/ 0.1uf AC coupled	USB 3.0 OTG Super Speed Transmit Negative.
S65	USB3_SSRX+	USB1_RX_P	USB1_RX_P/ A9	I, USB SS	USB 3.0 OTG Super Speed Receive Positive.
S66	USB3_SSRX-	USB1_RX_N	USB1_RX_N/ B9	I, USB SS	USB 3.0 OTG Super Speed Receive Negative.
S68	USB3+	USB_OTG1_DP	USB1_D_P/ D10	IO, USB	USB 2.0 OTG High Speed Data Positive.
S69	USB3-	USB_OTG1_DM	USB1_D_N/ E10	IO, USB	USB 2.0 OTG High Speed Data Negative.
P74	USB3_EN_OC#	USB1_OTG_OC(GPIO1_IO13)	GPIO1_IO13/ A6	I, 3.3V CMOS	USB OTG Power Enable/ Over Current Indicator.
S104	USB3_OTG_ID	USB_OTG1_ID	USB1_ID/ B11	I, 3.3V CMOS	NC. Optionally connected to USB OTG ID.

2.7.5 USB3.0 Host Interface

The i.MX 8M Plus SMARC SOM supports one USB 3.0 Host interface on SMARC PCB Edge connector. i.MX 8M Plus SoC's USB OTG2 controller with integrated USB3.0 MAC & PHY is used for USB3.0 Host interface The USB3.0 lanes are directly connected to USB2 port of SMARC PCB Edge connector. This USB3.0 OTG controller is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports USB dual-role operation but configured as host only to match the SMARC specification of USB2 port. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

To support USB 2.0 Host interface on this USB3.0 Host Interface port, i.MX 8M Plus SoC's USB OTG2 controller with integrated USB 2.0 MAC & PHY is used. This USB2.0 PHY output is connected to USB2 port of SMARC PCB Edge connector through four-port USB hub "USB2514" from Microchip. The Hub is used to support more USB2.0 Host Ports on SMARC PCB Edge connector.

For more details on USB 3.0 Host pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P69	USB2+	USB_HUB2OUT_DP	NA	IO, USB	USB 2.0 Port2 Data Positive. *Note: This pin is connected from 4port USB Hub Out2.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P70	USB2-	USB_HUB2OUT_DM	NA	IO, USB	USB 2.0 Port2 Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
P71	USB2_EN_OC#	USB_HUB2_OC	NA	I, 3.3V CMOS/ 10K PU	USB Port2 Power Enable/ Over Current Indicator. *Note: This pin is connected to USB Hub.*
S71	USB2_SSTX+	USB2_TX_P	USB2_TX_P/ A13	O, USB SS/ 0.1uf AC coupled	USB 3.0 Port2 Transmit Positive.
S72	USB2_SSTX-	USB2_TX_N	USB2_TX_N/ B13	O, USB SS/ 0.1uf AC coupled	USB 3.0 Port2 Transmit Negative.
S74	USB2_SSRX+	USB2_RX_P	USB2_RX_P/ A12	I, USB SS	USB 3.0 Port2 Receive Positive.
S75	USB2_SSRX-	USB2_RX_N	USB2_RX_N/ B12	I, USB SS	USB 3.0 Port2 Receive Negative.

2.7.6 USB 2.0 OTG Interface (Optional)

The i.MX 8M Plus SMARC SOM can optionally support USB2.0 OTG through the USB0 port of SMARC PCB Edge connector. The USB2.0 lines of the USB OTG2 controller (with integrated PHY) which supports USB2.0 High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfer is by default connected to the USB3 port of the SMARC Edge Connector where USB3.0 support is available for backward compatibility. When this support is made available, USB2.0 backward compatibility will be removed from the USB3 port of SMARC Edge.

For more details on USB 2.0 OTG pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P60	USB0+	USB0_DP	USB1_D_P/D10	IO, USB	Default NC. *Note: This pin is optionally connected from i.MX 8M Plus SoC USB1 Data Positive for USB 2.0 OTG through resistor and default not populated.* *Note: USB1 Data Positive is by default connected to S68th pin through resistor and default populated.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P61	USB0-	USB0_DM	USB1_D_N/E 10	IO, USB	Default NC. *Note: This pin is optionally connected from i.MX 8M Plus SoC USB1 Data Negative for USB 2.0 OTG through resistor and default not populated.* *Note: USB1 Data Negative is by default connected to S69th pin through resistor and default populated.*
P62	USB0_EN_OC#	USB0_EN_OC	GPIO1_IO13/ A6	IO, 3.3V CMOS	Default NC. *Note: This pin is optionally connected to GPIO1_IO13 through resistor and default not populated.*
P63	USB0_VBUS_DE T	VBUS_OTG1	USB1_VBUS/ A11	5V, Power	Default NC. *Note: This pin is optionally connected to i.MX 8M Plus SoC's USB1_VBUS for VBUS detection through resistor and default not populated.* *Note: Same power is also connected to SMARC Edge S37th pin through resistor and default populated.*
P64	USB0_OTG_ID	NC	NA	I, 3.3V CMOS	Default NC. *Note: This pin is optionally connected to i.MX 8M Plus SoC's USB1_ID pin through resistor and default not populated.*

Note: In default configuration USB2.0 lines of the OTG1 controller is connected to the USB3port of the SMARC Edge Connector. To support USB2.0 OTG on USB0 port of SMARC Edge, contact iWave Support team or refer Application Note: "AN4002-i.MX 8M PLUS SMARC SOM-Enabling USB 2.0 OTG Support in SMARC Edge-Application Note-R2.0-REL1.0.pdf".

2.7.7 USB 2.0 Host Interface

The i.MX 8M Plus SMARC SOM supports four USB2.0 Host interface on SMARC PCB Edge connector. To support four USB2.0 Host interfaces, SOM includes a four-port USB hub "USB2514" from Microchip. This Hub is interfaced with USB

OTG2 controller of i.MX 8M Plus SoC (with integrated PHY) which supports USB2.0 High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfer. This Hub output is directly connected to USB1, USB2, USB4 & USB5 ports of SMARC PCB Edge connector. The USB2 port of the SMARC Edge Connector supports USB3.0 and has the USB2.0 lines support available from the HUB for backwards compatibility.

For more details on USB 2.0 Host pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P65	USB1+	USB_HUB1OUT_DP	NA	IO, USB	USB 2.0 Port1 Data Positive. *Note: This pin is connected from 4port USB Hub Out1.*
P66	USB1-	USB_HUB1OUT_DM	NA	IO, USB	USB 2.0 Port1 Data Negative. *Note: This pin is connected from 4port USB Hub Out1.*
P67	USB1_EN_OC#	USB_HUB1_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port1 Over Current Indicator. *Note: This pin is connected to USB Hub OCS1 pin.*
P76	USB4_EN_OC#	USB_HUB3_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port3 Over Current Indicator. *Note: This pin is connected to USB Hub OCS3 pin.*
S35	USB4+	USB_HUB3OUT_DP	NA	IO, USB	USB 2.0 Port3 Data Positive. *Note: This pin is connected from 4port USB Hub Out3.*
S36	USB4-	USB_HUB3OUT_DM	NA	IO, USB	USB 2.0 Port3 Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
S55	USB5_EN_OC#	USB_HUB4_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port4 Over Current Indicator. *Note: This pin is connected to USB Hub OCS4 pin.*
S59	USB5+	USB_HUB4OUT_DP	NA	IO, USB	USB 2.0 Port4 Data Positive. *Note: This pin is connected from 4port USB Hub Out4.*
S60	USB5-	USB_HUB4OUT_DM	NA	IO, USB	USB 2.0 Port4 Data Negative. *Note: This pin is connected from 4port USB Hub Out4.*

2.7.8 PCIe Interface

The i.MX 8M Plus SMARC SOM supports one PCIe Gen3 lane on SMARC PCB Edge connector. i.MX 8M Plus SoC's PCIe 1 Controller with integrated PHY is directly connected to PCIe Link A port of SMARC PCB Edge connector. Optional 100MHz external clock oscillator output is available On-SOM, which will be connected to SoC & SMARC PCB Edge for PCIe reference clock. By default, internal PCIe Reference Clock is used. Also, PCIe reset and PCIe wake features are supported on SMARC PCB Edge connector using i.MX 8M Plus SoC IOs GPIO1_12 & GPIO1_14 respectively.

Note: PCIe differential transmitter lines are ac coupled on SOM itself. Also, when using PCIe differential clock lines from external clock oscillator no external termination is required as they are having On-SOM termination resistors.

For more details on PCIe pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P75	PCIE_A_RST#	GPIO_PCIE_RST(GPIO1_IO12)	GPIO1_IO12/ A5	O, 3.3V CMOS	PCIe Channel-A Reset Out.
P78	PCIE_A_CKREQ#	PCIE_CLKREQ_B	NA	I,3.3V CMOS	NC. *Note: Optionally connected to Enable of PCIe Clock Generator. Optional 10K PU and also optionally connected to GPIO5_02(SAI3_MCLK).*
P83	PCIE_A_REFCK+	PCIE_REFCLK_DP	PCIE_REF_PAD_CLK_P/D16	O, PCIe	PCIe Channel-A Clock Positive. *Note: This clock can also be optionally supplied using External Oscillator.*
P84	PCIE_A_REFCK-	PCIE_REFCLK_DM	PCIE_REF_PAD_CLK_N/E16	O, PCIe	PCIe Channel-A Clock Negative. *Note: This clock can also be optionally supplied using External Oscillator.*
P86	PCIE_A_RX+	PCIE_RXN_P	PCIE_RXN_P/ A14	I, PCIe	PCIe Channel-A Receive Positive.
P87	PCIE_A_RX-	PCIE_RXN_N	PCIE_RXN_N /B14	I, PCIe	PCIe Channel-A Receive Negative.
P89	PCIE_A_TX+	PCIE_TXN_P	PCIE_TXN_P/ A15	O, PCIe / 0.1µF AC Couple	PCIe Channel-A Transmit Positive.
P90	PCIE_A_TX-	PCIE_TXN_N	PCIE_TXN_N /B15	O, PCIe / 0.1µF AC Couple	PCIe Channel-A Transmit Negative.

2.7.9 MIPI CSI Interface

The i.MX 8M Plus SoC supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol

Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy-to-use pixel-based interface that supports 1 to 4 virtual channels and all data types. The i.MX 8M Plus SoC also supports 2 x ISP for providing aggregate performance and HDR processing.

The i.MX 8M Plus SMARC SOM supports one two lane and one four lane MIPI CSI camera interface via SMARC Edge connector along with the other control signals. Here all CSI2 lane [3:0] are connected to CSI1 port of the SMARC edge connector, but only CSI1 lane [1:0] are connected to CSI0 port of SMARC edge connector. This is due to the CSI0 port being 2 lanes as per the SMARC specification. MIPI CSI1 lane [3:0] are optionally connected to the On-SOM MIPI CSI Camera Connector.

For more details on MIPI CSI1 SMARC pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S5	CSI0_TX- / I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/ AJ7	O, 1.8V CMOS/ 4.7K PU	MIPI CSI1 I2C Clock.
S6	CAM_MCK	CAMERA_CCMCLKO1 (ECSPI2_MISO)	ECSPI2_MISO/ AH20	O, 1.8V CMOS	Master Clock for Camera.
S7	CSI0_TX+ / I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/ AJ6	IO, 1.8V CMOS/ 4.7K PU	MIPI CSI1 I2C Data.
S8	CSI0_CK+	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ D22	I, MIPI	MIPI CSI0 differential Clock positive.
S9	CSI0_CK	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ E22	I, MIPI	MIPI CSI0 differential Clock negative.
S11	CSI0_RX0+	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P/ D18	I, MIPI	MIPI CSI0 differential data lane 0 positive.
S12	CSI0_RX0-	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N/ E18	I, MIPI	MIPI CSI0 differential data lane 0 negative.
S14	CSI0_RX1+	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P/ D20	I, MIPI	MIPI CSI0 differential data lane 1 positive.
S15	CSI0_RX1-	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N/ E20	I, MIPI	MIPI CSI0 differential data lane 1 negative.

For more details on MIPI CSI2 SMARC pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	CSI1_TX+ / I2C_CAM1_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, 1.8V CMOS/ 4.7K PU	MIPI CSI2 I2C Clock.
S2	CSI1_TX- / I2C_CAM1_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, 1.8V CMOS/	MIPI CSI2 I2C Data.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
				4.7K PU	
P3	CSI1_CK+	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P/ A23	I, MIPI	MIPI CSI2 differential clock positive.
P4	CSI1_CK-	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N/ B23	I, MIPI	MIPI CSI2 differential clock negative.
P7	CSI1_RX0+	MIPI_CSI2_D0_P	MIPI_CSI2_D0_P/ A25	I, MIPI	MIPI CSI2 differential data lane 0 positive.
P8	CSI1_RX0-	MIPI_CSI2_D0_N	MIPI_CSI2_D0_N/ B25	I, MIPI	MIPI CSI2 differential data lane 0 negative.
P10	CSI1_RX1+	MIPI_CSI2_D1_P	MIPI_CSI2_D1_P/ A24	I, MIPI	MIPI CSI2 differential data lane 1 positive.
P11	CSI1_RX1-	MIPI_CSI2_D1_N	MIPI_CSI2_D1_N/ B24	I, MIPI	MIPI CSI2 differential data lane 1 negative.
P13	CSI1_RX2+	MIPI_CSI2_D2_P	MIPI_CSI2_D2_P/ A22	I, MIPI	MIPI CSI2 differential data lane 2 positive.
P14	CSI1_RX2-	MIPI_CSI2_D2_N	MIPI_CSI2_D2_N/ B22	I, MIPI	MIPI CSI2 differential data lane 2 negative.
P16	CSI1_RX3+	MIPI_CSI2_D3_P	MIPI_CSI2_D3_P/ A21	I, MIPI	MIPI CSI2 differential data lane 3 positive.
P17	CSI1_RX3-	MIPI_CSI2_D3_N	MIPI_CSI2_D3_N/ B21	I, MIPI	MIPI CSI2 differential data lane 3 negative.

2.7.10 HDMI TX Interface

The i.MX 8M Plus SMARC SOM supports one HDMI Interface on SMARC PCB Edge connector. i.MX 8M Plus SoC's HDMI Display Transmitter Controller with integrated PHY is directly connected to HDMI port of SMARC PCB Edge connector. It supports dedicated DDC interface on SMARC PCB Edge connector for HDMI EDID read and to carry the HDCP & SCDC commands. i.MX 8M Plus SoC supports HDMI 1.4 Specification & HDMI 2.0a (3840 x 2160p30) Specification. The SoC inbuilt PHY also supports 32 channel audio output support. The HDMI TX PHY of the i.MX 8M Plus SoC supports pixel clock frequency of up to 297MHz.

For more details on HDMI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P92	HDMI_D2+ / DP1_LANE0+	HDMI_TX_D2_P	HDMI_TX2_P/AH27	O, HDMI	HDMI differential data lane 2 Positive
P93	HDMI_D2- / DP1_LANE0-	HDMI_TX_D2_N	HDMI_TX2_N/AJ27	O, HDMI	HDMI differential data lane 2 Negative
P95	HDMI_D1+ / DP1_LANE1+	HDMI_TX_D1_P	HDMI_TX1_P/AH26	O, HDMI	HDMI differential data lane 1 Positive
P96	HDMI_D1- / DP1_LANE1-	HDMI_TX_D1_N	HDMI_TX1_N/AJ26	O, HDMI	HDMI differential data lane 1 Negative
P98	HDMI_D0+ / DP1_LANE2+	HDMI_TX_D0_P	HDMI_TX0_P/AH25	O, HDMI	HDMI differential data lane 0 Positive

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P99	HDMI_D0- / DP1_LANE2-	HDMI_TX_D0_N	HDMI_TX0_N/AJ25	O, HDMI	HDMI differential data lane 0 Negative
P101	HDMI_CK+ / DP1_LANE3+	HDMI_TX_CLK_P	HDMI_TXC_P/AH24	O, HDMI	HDMI differential CLK Positive
P102	HDMI_CK- / DP1_LANE3-	HDMI_TX_CLK_N	HDMI_TXC_N/AJ24	O, HDMI	HDMI differential CLK Negative
P104	HDMI_HPD / DP1_HPD	HDMI_TX_HPD	HDMI_HPD/AE22	I, 1.8V CMOS/ 1M PD	HDMI Hot Plug Detect
P105	HDMI_CTRL_CK / DP1_AUX+	HDMI_TX_DDC_SCL	HDMI_DDC_SCL/AC22	IO, 1.8V CMOS/ 100K PU	HDMI DDC I2C Clock
P106	HDMI_CTRL_DAT / DP1_AUX	HDMI_TX_DDC_SDA	HDMI_DDC_SDA/AF22	IO, 1.8V CMOS/ 100K PU	HDMI DDC I2C DATA

2.7.11 MIPI DSI Display Interface

SMARC Specification supports two display interfaces over edge connector, which can be either LVDS or MIPI DSI display. The i.MX 8M Plus SoC supports single MIPI DSI and two LVDS display channels. The MIPI DSI interface from the i.MX 8M Plus SoC is by default connected to the Display Channel0 of the SMARC PCB Edge Connector.

The i.MX 8M Plus SoC MIPI_DSI standard controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

An option is provided on i.MX 8M Plus SMARC SOM to support either LVDS0 or MIPI DSI1 over the edge connector for Display Channel0 and in default configuration MIPI DSI1 is supported.

For more details on DSI pinouts on Display Controller 0 of SMARC PCB Edge Connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0/DSI0_D0_P	MIPI_DSI1_D0_P/ A16	O, MIPI	MIPI DSI1 differential data lane 0 positive *Note: Optionally connected to LVDS0 differential data lane 0 positive*
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0/DSI0_D0_N	MIPI_DSI1_D0_N/ B16	O, MIPI	MIPI DSI1 differential data lane 0 negatives

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Optionally connected to LVDS0 differential data lane 0 negative
S127	LCD0_BKLT_EN	LCD0_BKLT_EN_GPIO3_7 (NAND_DATA01)	NAND_DATA01/ L25	O, 1.8V CMOS	LCD0 Backlight Enable
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0/DSI0_D1_P	MIPI_DSI1_D1_P/ A17	O, MIPI	MIPI DSI1 differential data lane 1 positive *Note: Optionally connected to LVDS0 differential data lane 1 positive*
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0/DSI0_D1_N	MIPI_DSI1_D1_N/ B17	O, MIPI	MIPI DSI1 differential data lane 1 negative *Note: Optionally connected to LVDS0 differential data lane 1 negative*
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0/DSI0_D2_P	MIPI_DSI1_D2_P/ A19	O, MIPI	MIPI DSI1 differential data lane 2 positive *Note: Optionally connected to LVDS0 differential data lane 2 positive*
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0/DSI0_D2_N	MIPI_DSI1_D2_N/ B19	O, MIPI	MIPI DSI1 differential data lane 2 negative *Note: Optionally connected to LVDS0 differential data lane 2 negative*
S133	LCD0_VDD_EN	LCD0_VDD_EN_GPIO3_8 (NAND_DATA02)	NAND_DATA02/ L24	O, 1.8V CMOS	LCD0 Power Enable
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0/DSI0_CLK_P	MIPI_DSI1_CLK_P/ A18	O, MIPI	MIPI DSI1 differential Clock positive *Note: Optionally connected to LVDS0 differential Clock positive*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0/DSI0_CLK_N	MIPI_DSI1_CLK_N/ B18	O, MIPI	MIPI DSI1 differential Clock negative *Note: Optionally connected to LVDS0 differential Clock negative*
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0/DSI0_D3_P	MIPI_DSI1_D3_P/ A20	O, MIPI	MIPI DSI1 differential data lane 3 positive *Note: Optionally connected to LVDS0 differential data lane 3 positive*
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0/DSI0_D3_N	MIPI_DSI1_D3_N/ B20	O, MIPI	MIPI DSI1 differential data lane 3 negative *Note: Optionally connected to LVDS0 differential data lane 3 negative*
S139	I2C_LCD_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, 1.8V CMOS/ 4.7K PU	I2C CLK for Display and Touch
S140	I2C_LCD_DAT	I2C5_SDA(SPDIF_RX	SPDIF_RX/ AD18	IO, 1.8V CMOS/ 4.7K PU	I2C DATA for Display and Touch
S141	LCD0_BKLT_PWM	PWM1_OUT(I2C4_SDA)	I2C4_SDA/ AD8	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM

2.7.12 MIPI LVDS Display Interface

In the i.MX8M Plus SOM the LVDS0 controller of the SoC is optionally connected to Display Channel0 of the SMARC PCB Edge Connector and LVDS1 is by default connected to the Display Channel1 of the SMARC PCB Edge Connector.

The i.MX 8M Plus SoC supports two LDB to support the synchronous flow of RGB data to external display through the LVDS interface. The LVDS controller can support single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock for which either LVDS0 or LVDS1 can be used. By using both LVDS0 and LVDS Dual asynchronous channels (8 data, 2 clocks), it can support upto 160MHz pixel clock with resolutions above 1366x768p60, up to 1080p60.

For more details on LVDS0 pinouts on Display Controller0 of SMARC PCB Edge Connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S125	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0/DSI0_D0_P	LVDS0_D0_P/ D29	O, MIPI	By default, connected to MIPI DSI1 differential data lane 0 positive. *Optionally connected to LVDS0 differential data lane 0 positive*
S126	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0/DSI0_D0_N	LVDS0_D0_N/ E28	O, MIPI	By default, connected to MIPI DSI1 differential data lane 0 negatives. *Optionally connected to LVDS0 differential data lane 0 negative*
S127	LCD0_BKLT_EN	LCD0_BKLT_EN_GPIO3_7 (NAND_DATA01)	NAND_DATA01/ L25	O, 1.8V CMOS	LCD0 Backlight Enable
S128	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0/DSI0_D1_P	LVDS0_D1_P/ E29	O, MIPI	By default, connected to MIPI DSI1 differential data lane 1 positive. *Optionally connected to LVDS0 differential data lane 1 positive*
S129	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0/DSI0_D1_N	LVDS0_D1_N/ F28	O, MIPI	By default, connected to MIPI DSI1 differential data lane 1 negative. *Optionally connected to LVDS0 differential data lane 1 negative*
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0/DSI0_D2_P	LVDS0_D2_PP/ G29	O, MIPI	By default, connected to MIPI DSI1 differential data lane 2 positive. *Optionally connected to*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					LVDS0 differential data lane 2 positive
S132	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0/DSI0_D2_N	LVDS0_D2_N/ H28	O, MIPI	By default, connected to MIPI DSI1 differential data lane 2 negative. *Optionally connected to LVDS0 differential data lane 2 negative*
S133	LCD0_VDD_EN	LCD0_VDD_EN_GPIO3_8 (NAND_DATA02)	NAND_DATA02/ L24	O, 1.8V CMOS	LCD0 Power Enable
S134	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0/DSI0_CLK_P	LVDS0_CLK_P/ F29	O, MIPI	By default, connected to MIPI DSI1 differential Clock positive. *Optionally connected to LVDS0 differential Clock positive*
S135	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0/DSI0_CLK_N	LVDS0_CLK_N/ G28	O, MIPI	By default, connected to MIPI DSI1 differential Clock negative. *Optionally connected to LVDS0 differential Clock negative*
S137	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0/DSI0_D3_P	LVDS0_D3_P/ H29	O, MIPI	By default, connected to MIPI DSI1 differential data lane 3 positive. *Optionally connected to LVDS0 differential data lane 3 positive*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S138	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0/DSI0_D3_N	LVDS0_D3_N/ J28	O, MIPI	By default, connected to MIPI DSI1 differential data lane 3 negative. *Optionally connected to LVDS0 differential data lane 3 negative*
S139	I2C_LCD_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, 1.8V CMOS/ 4.7K PU	I2C CLK for Display and Touch
S140	I2C_LCD_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, 1.8V CMOS/ 4.7K PU	I2C DATA for Display and Touch
S141	LCD0_BKLT_PWM	PWM1_OUT(I2C4_SDA)	I2C4_SDA/ AD8	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM

Note: Contact iWave support team if LVDS0 supported SOM is required or refer Application note: "AN4001-i.MX 8M PLUS SMARC SOM-Enabling LVDS Support in SMARC Edge-Application Note-R2.0-REL1.0.pdf"

For more details on LVDS1 pinouts on Display Controller1 of SMARC PCB Edge Connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S107	LCD1_BKLT_EN	LCD1_BKLT_EN_GPIO3_14 (NAND_DQS)	NAND_DQS/ R26	O, 1.8V CMOS	LCD1 Backlight Enable
S108	LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	LVDS1_CLK_P/ A28	O, LVDS	LVDS1 differential Clock positive
S109	LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	LVDS1_CLK_N/ B28	O, LVDS	LVDS1 differential Clock negative
S111	LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P	LVDS1_D0_P/ A26	O, LVDS	LVDS1 differential data lane 0 positive
S112	LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N	LVDS1_D0_N/ B26	O, LVDS	LVDS1 differential data Lane 0 negative
S114	LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P	LVDS1_D1_P/ A27	O, LVDS	LVDS1 differential data lane 1 positive
S115	LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N	LVDS1_D1_N/ B27	O, LVDS	LVDS1 differential data lane 1 negative
S116	LCD1_VDD_EN	LCD1_VDD_EN_GPIO3_28 (HDMI_CEC)	HDMI_CEC/ AD22	O, 1.8V CMOS	LCD1 Power Enable

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S117	LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P	LVDS1_D2_P/ B29	O, LVDS	LVDS1 differential data lane 2 positive
S118	LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N	LVDS1_D2_N/ C28	O, LVDS	LVDS1 differential data lane 2 negative
S120	LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P	LVDS1_D3_P/ C29	O, LVDS	LVDS1 differential data lane 3 positive
S121	LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N	LVDS1_D3_N/ D28	O, LVDS	LVDS1 differential data lane 3 negative
S122	LCD1_BKLT_PWM	PWM2_OUT(SAI5_RXD0)	SAI5_RXD0/ AE16	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM

2.7.13 Audio Interface

The i.MX 8M Plus SMARC SOM supports I2S0 and I2S1 channels of SMARC Edge connector from SoC's SAI2 and SAI3 channels respectively. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and supports 49.152 MHz BCLK. Only Transmitter Clock and Transmitter Left-Right Clock (LRCK) is supported as per SMARC specification.

In i.MX 8M Plus SMARC SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on SMARC Edge I2S pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S38	AUDIO_MCK	SAI2_MCLK	SAI2_MCLK/ AJ15	O, 1.8V CMOS	Master Clock for Audio codec
S39	I2S0_LRCK	SAI2_TX_SYNC(SAI2_TXFS)	SAI2_TXFS/ AJ17	O, 1.8V CMOS	Serial Audio Interface Channel1 Frame Sync /Left Right Clock
S40	I2S0_SDOUT	SAI2_TX_DATA0(SAI2_TXD0)	SAI2_TXD0/ AH16	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
S41	I2S0_SDIN	SAI2_RX_DATA0(SAI2_RXD0)	SAI2_RXD0/ AJ14	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
S42	I2S0_CK	SAI2_TX_BCLK(SAI2_TXC)	SAI2_TXC/ AH15	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel1 Clock
S50	HDA_SYNC / I2S2_LRCK	SAI3_TX_SYNC(SAI3_TXFS)	SAI3_TXFS/ AC16	O, 1.8V CMOS	Serial Audio Interface Channel0 Left Right Clock
S51	HDA_SDO / I2S2_SDOUT	SAI3_TX_DATA0(SAI3_TXD)	SAI3_TXD/ AH18	O, 1.8V CMOS	Serial Audio Interface Channel0 Data Output
S52	HDA_SDI / I2S2_SDIN	SAI3_RX_DATA0(NAND_DATA00)	NAND_DATA00/ R25	I, 1.8V CMOS	Serial Audio Interface Channel0 Data Input
S53	HDA_CK / I2S2_CK	SAI3_TX_BCLK(SAI3_TXC)	SAI3_TXC/ AH19	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel0 Clock

2.7.14 SPI Interface

The i.MX 8M Plus SoC supports enhanced Configurable Serial Peripheral Interface (ECSPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum data rate of 52 Mbits/s. The i.MX 8M Plus SMARC SOM supports SPI0 and SPI1 channels of the SMARC Edge connector using ECSPI1 and ECSPI2 of SoC.

For more details on SPI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P43	SPI0_CS0#	ECSPI1_SS0	ECSPI1_SS0/ AE20	O, 1.8V CMOS	SPI0 Chip Select 0
P44	SPI0_CK	ECSPI1_SCLK	ECSPI1_SCLK/ AF20	O, 1.8V CMOS/ 33E Series	SPI0 Clock
P45	SPI0_DIN	ECSPI1_MISO	ECSPI1_MISO/ AD20	I, 1.8V CMOS	SPI0 Master IN Slave Out
P46	SPI0_DO	ECSPI1_MOSI	ECSPI1_MOSI/ AC20	O, 1.8V CMOS	SPI0 Master Out Slave In
P54	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0	ECSPI2_SS0/ AJ22	O, 1.8V CMOS	SPI1 Chip Select 0
P56	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK	ECSPI2_SCLK/ AH21	O, 1.8V CMOS/ 33E Series	SPI1 Clock
P57	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (I2C4_SCL)	I2C4_SCL/ AF8	I, 1.8V CMOS	SPI1 Master IN Slave Out
P58	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI	ECSPI2_MOSI/ AJ21	O, 1.8V CMOS	SPI1 Master Out Slave In

2.7.15 Data UART

SMARC V2.1.1 supports four UART channels where two channels SER0 & SER2 are with CTS and RTS and two channels SER1 & SER3 are without. The i.MX 8M Plus SoC's UART2 and UART3 connected SER0 and SER1 channels of SMARC Edge connector respectively. Whereas SER2 channel of SMARC Edge connector optionally connected to UART1 of i.MX 8M Plus SoC. In default configuration UART1 is connected to on SOM Bluetooth module. SER1 of the SMARC Edge connector is optionally connected to the on-SOM GNSS Module. SER0, SER1 & SER2 can be used for any data communication. UART4 of the SoC is connected to SER3 channel of SMARC Edge connector and used as Debug UART.

For more details on UART pinouts, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P129	SER0_TX	UART2_TXD	UART2_TXD/ AH4	O, 1.8V CMOS	UART2 Transmitter.
P130	SER0_RX	UART2_RXD	UART2_RXD/ AF6	I, 1.8V CMOS	UART2 Receiver.
P131	SER0_RTS#	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/ AJ18	O, 1.8V CMOS	UART2 Request to Send.
P132	SER0_CTS#	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/ AF18	I, 1.8V CMOS	UART2 Clear to Send.
P134	SER1_TX	UART3_TXD	NAND_CE0_B/ L26	O, 1.8V CMOS	UART3 Transmitter.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P135	SER1_RX	UART3_RXD	NAND_ALE/ N25	I, 1.8V CMOS	UART3 Receiver.
P136	SER2_TX	UART1_TX	UART1_TXD/ AJ3	O, 1.8V CMOS	NC. *Note: Optionally connect to UART1_TX. By default, connected to on SOM Bluetooth module.*
P137	SER2_RX	UART1_RX	UART1_RXD/ AD6	I, 1.8V CMOS	NC. *Note: Optionally connect to* UART1_RX. *By default, connected to on SOM Bluetooth module.*
P138	SER2_RTS#	UART1_CTS_B	UART3_RXD/ AE6	O, 1.8V CMOS	NC. *Note: Optionally connect to* UART1_CTS_B. *By default, connected to on SOM Bluetooth module.*
P139	SER2_CTS#	UART1_RTS_B	UART3_TXD/ AJ4	I, 1.8V CMOS	NC. *Note: Optionally connect to* UART1_RTS_B. *By default, connected to on SOM Bluetooth module.*
P140	SER3_TX	UART4_TX	UART4_TXD/ AH5	O, 1.8V CMOS	Debug UART Transmitter. *Note: Optionally connected to on SOM Debug Header.*
P141	SER3_RX	UART4_RX	UART4_RXD/ AJ5	I, 1.8V CMOS	Debug UART Receiver. *Note: Optionally connected to on SOM Debug Header.*

2.7.16 SMARC GPIOs

SMARC V2.1.1 supports 14 GPIOs, which can be used for any general-purpose application and are listed below. But, if extra GPIO are required then refer **"i.MX 8M Plus Pin Multiplexing on SMARC Edge"** table, which gives all optional GPIO supported via Edge connector.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P108	GPIO0 / CAM0_PWR #	SMARC_GPIO_0_GPIO4_18(SAI1_TXD6)	SAI1_TXD6/AC12	IO, 1.8V CMOS	SMARC General Purpose Input/output 0.

P109	GPIO1 / CAM1_PWR #	SMARC_GPIO_1_GPIO4_19(SAI1_TXD7)	SAI1_TXD7/AJ13	IO, 1.8V CMOS	SMARC General Purpose Input/output 1.
P110	GPIO2 / CAM0_RST#	SMARC_GPIO_2_GPIO4_0(SAI1_RXFS)	SAI1_RXFS/AJ9	IO, 1.8V CMOS	SMARC General Purpose Input/output 2.
P111	GPIO3 / CAM1_RST#	SMARC_GPIO_3_GPIO4_1(SAI1_RXC)	SAI1_RXC/AH8	IO, 1.8V CMOS	SMARC General Purpose Input/output 3.
P112	GPIO4 / HDA_RST#	SMARC_GPIO_4_GPIO4_2(SAI1_RXD0)	SAI1_RXD0/AC10	IO, 1.8V CMOS	SMARC General Purpose Input/output 4.
P113	GPIO5 / PWM_OUT	SMARC_GPIO_5_GPIO3_20(SAI5_RXC)	SAI5_RXC/AD14	IO, 1.8V CMOS	SMARC General Purpose Input/output 5.
P114	GPIO6 / TACHIN	SMARC_GPIO_6_GPIO4_22(SAI2_RXC)	SAI2_RXC/AJ16	IO, 1.8V CMOS	SMARC General Purpose Input/output 6.
P115	GPIO7	SMARC_GPIO_7_GPIO4_21(SAI2_RXFS)	SAI2_RXFS/AH17	IO, 1.8V CMOS	SMARC General Purpose Input/output 7.
P116	GPIO8	SMARC_GPIO_8_GPIO4_28(SAI3_RXFS)	SAI3_RXFS/AJ19	IO, 1.8V CMOS	SMARC General Purpose Input/output 8.
P117	GPIO9	SMARC_GPIO_9_GPIO4_3(SAI1_RXD1)	SAI1_RXD1/AF10	IO, 1.8V CMOS	SMARC General Purpose Input/output 9.
P118	GPIO10	SMARC_GPIO_10_GPIO3_21(SAI5_RXFS)	SAI5_RXFS/AC14	IO, 1.8V CMOS	SMARC General Purpose Input/output 10.

P119	GPIO11	SMARC_GPIO_11_GPIO5_5(SPDIF1_EXT_CLK)	SPDIF_EXT_CLK / AC18	IO, 1.8V CMOS	SMARC General Purpose Input/output 11.
S123	GPIO13	SMARC_GPIO_13_GPIO3_28(HDMI_CEC)	HDMI_CEC/AD22	IO, 1.8V CMOS	NC (Optionally SMARC General Purpose Input/output 13).
S142	GPIO12	SMARC_GPIO_12_GPIO3_21(NAND_DQS)	NAND_DQS/R26	IO, 1.8V CMOS	NC (Optionally SMARC General Purpose Input/output 12).

2.7.17 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0B protocol specifications.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module.

The i.MX 8M Plus SOC Supports two CAN interface and are connected to SMARC Edge Connector.

For more details of CAN pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P143	CAN0_TX	FLEXCAN1_TX(SAI5_RXD1)	SAI5_RXD1/ AD16	O, 1.8V CMOS	CAN 1 Transmitter.
P144	CAN0_RX	FLEXCAN1_RX(SAI5_RXD2)	SAI5_RXD2/ AF16	I, 1.8V CMOS	CAN 1 Receiver.
P145	CAN1_TX	FLEXCAN2_TX(SAI5_RXD3)	SAI5_RXD3/ AE14	O, 1.8V CMOS	CAN 2 Transmitter.
P146	CAN1_RX	FLEXCAN2_RX(SAI5_MCLK)	SAI5_MCLK/ AF14	I, 1.8V CMOS	CAN 2 Receiver.

2.7.18 I2C Interface

SMARC Specification V2.1.1 supports Five I2C but i.MX 8M Plus SOM supports only four I2C in default configuration and fifth I2C as optional which are listed down:

For more details of I2C pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	CSI1_TX+ / I2C_CAM1_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, 1.8V CMOS 4.7K PU	Secondary Camera Purpose I2C Clock.
S2	CSI1_TX- / I2C_CAM1_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, 1.8V CMOS 4.7K PU	Secondary Camera Purpose I2C Data.
S5	CSI0_TX- / I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/ AJ7	O, 1.8V CMOS 4.7K PU	Primary Camera Purpose I2C Clock.
S7	CSI0_TX+ / I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/ AJ6	IO, 1.8V CMOS 4.7K PU	Primary Camera Purpose I2C Clock.
S48	I2C_GP_CK	I2C2_SCL	I2C2_SCL/ AH6	O, 1.8V CMOS 4.7K PU	General Purpose I2C Clock.
S49	I2C_GP_DAT	I2C2_SDA	I2C2_SDA/ AE8	IO, 1.8V CMOS 4.7K PU	General Purpose I2C Data.
S139	I2C_LCD_CK	I2C5_SCL(SPDIF_TX)	SPDIF_TX/ AE18	O, 1.8V CMOS 4.7K PU	Display Purpose I2C Clock.
S140	I2C_LCD_DAT	I2C5_SDA(SPDIF_RX)	SPDIF_RX/ AD18	IO, 1.8V CMOS 4.7K PU	Display Purpose I2C Clock.
P121	I2C_PM_CK	*I2C1_SCL*	I2C1_SCL/ AC8	O, 1.8V CMOS 4.7K PU	NC. *Note: Optionally connected to I2C1_SCL-PMIC I2C*
P122	I2C_PM_DAT	*I2C1_SCL*	I2C1_SDA/ AH7	IO, 1.8V CMOS 4.7K PU	NC. *Note: Optionally connected to I2C1_SDA-PMIC I2C*

2.7.19 Control Signals

SMARC V2.1.1 specification supports control Signals, for more details on SMARC Control Signals pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P126	RESET_OUT#	GPIO_RESET_OUT_GPIO1_9_1V8	GPIO1_IO08/A8	I, 1.8V CMOS	RESET OUT from SoC to all other peripherals.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P127	RESET_IN#	PMIC_RST_B	NA	I, 1.8V CMOS 100K PU	Hard RESET Input to SOM.
P128	POWER_BTN#	CPU_ON_OFF	ONOFF/ G22	I, 1.8V CMOS 100K PU	Power ON /OFF Input to SOM.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	I, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier Board power supplies shall not be enabled while this signal is held low by the Carrier.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	O, 1.8V CMOS	Carrier Board power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	O, 1.8V CMOS 10K PU	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.
S157	TEST#	TEST#	NA	I, 1.8V CMOS	Not supported. *Note: This pin is connected to GND in SOM.*

2.7.20 Boot Select

The i.MX 8M Plus SMARC SOM supports three Boot Select pins as per SMARC V2.1.1 specification. i.MX 8M Plus SMARC SOM supports booting from On-SOM eMMC, SMARC SD (from carrier board) and eCSPI. Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

Boot Select Pins			Description
BOOT_SEL2#	**BOOT_SEL1#**	**BOOT_SEL0#**	
Float	Float	GND	eMMC Flash (uSDHC3)
GND	GND	Float	SMARC SD (uSDHC2)
GND	Float	Float	eCSPI

Also, i.MX 8M Plus SMARC SOM supports active low FORCE_RECOV# functionality as per SMARC V2.1.1 specification. Pulling low this pin forces the i.MX 8M Plus SoC to serial download mode where the SoC boot media can be programmed through i.MX 8M Plus SoC's USB1 controller USB 3.0 interface which is connected to USB3 port of SMARC PCB Edge connector.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P123	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 0
P124	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 1
P125	BOOT_SEL2#	BOOT_SEL2#	NA	I, 1.8V CMOS 10K PU	Boot Media Select bit 2
S155	FORCE_RECOV#	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Active low Force Recovery Input.

2.7.21 Power and GND

The i.MX 8M Plus SMARC SOM works with 5V power input (VCC) from SMARC PCB Edge Connector and generates all other required powers internally On-SOM itself. i.MX 8M Plus SMARC SOM also supports coin cell power input (VDD_RTC) from SMARC PCB Edge Connector to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
P147, P148, P149, P150, P151, P152, P153, P154, P155, P156	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage.
P2, P9, P12, P15, P18, P32, P38, P47, P50, P53, P59, P68, P79, P82, P85, P88, P91, P94, P97, P100, P103, P120, P133, P142, S3, S10, S13, S16, S25, S34, S47, S61, S64, S67, S70, S73, S80, S83, S86, S89, S92, S101, S110, S119, S124, S130, S136, S143, S158	GND	GND	NA	Power	Ground.
S147	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.8 Other Features

2.8.1 Fan Header

The i.MX 8M Plus SMARC SOM supports a Fan Header to connect cooling Fan if required. This Fan Header (J3) is physically located at the top of the board as shown below.

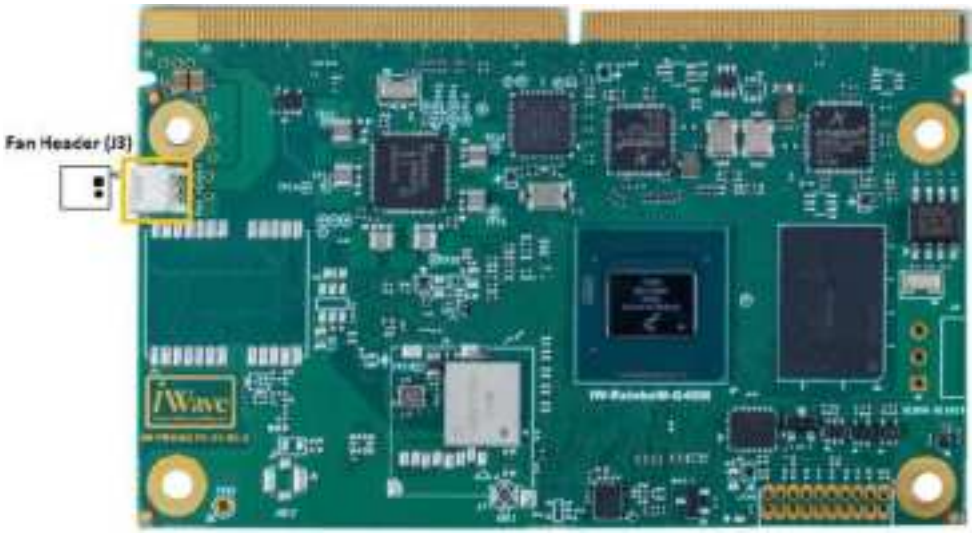


Figure 6: Fan Header

Number of Pins - 2

Connector Part - 53048-0210 from Molex

Mating Connector - 51021-0200 from Molex

Table 4: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.8.2 MIPI CSI Camera Connector (Optional)

The i.MX 8M Plus SoC supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core is compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy-to-use pixel-based interface that supports 1 to 4 virtual channels and all data types. The i.MX 8M Plus SoC also supports 2 x ISP for providing aggregate performance and HDR processing.

As the MIPI CSI0 interface of SMARC Edge only supports 2 lane MIPI CSI, so an optional 36 pin MIPI-CSI connector is supported on SOM supporting all 4 lanes of MIPI CSI1 controller of i.MX 8M Plus SoC.

Number of Pins : 36

Connector Part : FH12A-36S-0.5SH(55)

For more details on MIPI CSI1 pinouts on MIPI CSI Camera connector, refer below table:

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VDD_3V3	NA	Power	3V3 Camera Power
2	VDD_3V3	NA	Power	3V3 Camera Power
3	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P/ D18	I, MIPI	MIPI CSI1 differential data lane 0 positive.
4	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N/ E18	I, MIPI	MIPI CSI1 differential data lane 0 negative.
5	GND	NA	Power	Ground.
6	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P/ D20	I, MIPI	MIPI CSI1 differential data lane 1 positive.
7	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N/ E20	I, MIPI	MIPI CSI1 differential data lane 1 negative.
8	GND	NA	Power	Ground.
9	MIPI_CSI1_D2_P	MIPI_CSI1_D2_P/ D24	I, MIPI	MIPI CSI1 differential data lane 2 positive.
10	MIPI_CSI1_D2_N	MIPI_CSI1_D2_N/ E24	I, MIPI	MIPI CSI1 differential data lane 2 negative.
11	SMARC_GPIO_4_GPIO4_2	SAI1_RXD0/AC10	IO, 1.8V CMOS	MIPI Camera Reset signal
12	MIPI_CSI1_D3_P	MIPI_CSI1_D3_P/ D26	I, MIPI	MIPI CSI1 differential data lane 3 positive.
13	MIPI_CSI1_D3_N	MIPI_CSI1_D3_N/ E26	I, MIPI	MIPI CSI1 differential data lane 3 negative.
14	GND	NA	Power	Ground.
15	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ D22	I, MIPI	MIPI CSI1 differential Clock positive.

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
16	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ E22	I, MIPI	MIPI CSI1 differential Clock negative.
17	GND	NA	Power	Ground.
18	I2C3_SCL	I2C3_SCL/ AJ7	O, 1.8V CMOS/ 4.7K PU	I2C Clock for MIPI CSI1 Camera
19	I2C3_SDA	I2C3_SDA/ AJ6	IO, 1.8V CMOS/ 4.7K PU	I2C Data for MIPI CSI1 Camera
20	SMARC_GPIO_0_GPIO4_18(SAI1_TXD6)	SAI1_TXD6/AC12	IO, 1.8V CMOS	Camera 0 Enable (active low).
21	CAMERA_CCMCLKO1 (ECSPI2_MISO)	I2C4_SCL/ AF8	O, 1.8V CMOS	Master Clock for Camera
22	NC	NA	-	-
23	NC	NA	-	-
24	NC	NA	-	-
25	GND	NA	Power	Ground.
26	CKOUT1	CKOUT1/ K29	O, 1.8V CMOS	Clock Out from SoC.
27	CKOUT2	CKOUT2/ L29	O, 1.8V CMOS	Clock Out from SoC.
28	GND	NA	Power	Ground.
29	CLKIN1	CLKIN1/ K28	I, 1.8V CMOS	Clock In to SoC.
30	CLKIN2	CLKIN2/ L28	I, 1.8V CMOS	Clock In to SoC.
31	NC	NA	-	-
32	NC	NA	-	-
33	NC	NA	-	-
34	GND	NA	Power	Ground.
35	CAM0_GPIO	GPIO1_IO03/ D6	IO, 1.8V CMOS	GPIO for MIPI CSI1 Camera.
36	NC	NA	-	-

2.8.3 Debug UART Header (Optional)

The i.MX 8M Plus SMARC SOM optionally supports 3pin UART header for i.MX 8M Plus SoC's debug purpose. The i.MX 8M Plus SoC's UART4 can be connected to this header. FTDI's UART to USB smart cable (*TTL-232RG-VREG1V8)* can be directly connected between this header and Host PC for debugging. This UART header (J4) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Number of Pins - 3

Connector Part - M20-9960345 from Harwin Inc.

Table 5: Debug UART Header Pin Assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	UART4_TXD_CONN	UART4_TXD/AH5	O, 1.8V CMOS	Debug UART Transmitter
2	UART4_RXD_CONN	UART4_RXD/AJ5	I, 1.8V CMOS	Debug UART Receiver
3	GND	NA	Power	Ground

2.8.4 JTAG Header (Optional)

The i.MX 8M Plus SMARC SOM optionally supports JTAG interface for SoC debug purpose. A customized 20-pin ARM JTAG connector (J8) is available in SOM for JTAG interface. The i.MX 8M Plus SoC's JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector (J8) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Number of Pins - 20

Connector Part - GRPB102MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

Table 6: JTAG Header Pin Assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VDD_1V8	NA	O, 1.8V Power	VTREF Voltage Reference.
2	VFRE_JTAG1	NA	O, 1.8V Power	Supply Voltage.
3	-	NA	O, 1.8V CMOS/ 10K PU	Only pull up is provided.
4	GND	NA	Power	Ground.
5	JTAG_TDI	JTAG_TDI/ G16	I, 1.8V CMOS/ 10K PU	JTAG test data input.

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
6	GND	NA	Power	Ground.
7	JTAG_TMS	JTAG_TMS/ G14	I, 1.8V CMOS/ 10K PD	JTAG test mode select.
8	GND	NA	Power	Ground.
9	JTAG_TCK	JTAG_TCK/ G18	I, 1.8V CMOS/ 10K PU/PD	JTAG test Clock.
10	GND	NA	Power	Ground.
11	-	NA	-	Only pull down is provided.
12	GND	NA	Power	Ground.
13	JTAG_TDO	JTAG_TDO/ F14	O, 1.8V CMOS, 10K PU	JTAG test data output.
14	GND	NA	Power	Ground.
15	-	NA	O, 1.8V CMOS/ 10K PU	Only pull up is provided.
16	GND	NA	Power	Ground.
17	-	NA	-	Only pull up is provided.
18	GND	NA	Power	Ground.
19	-	NA	-	Only pull down is provided.
20	GND	NA	Power	Ground.

2.9 i.MX 8M Plus Pin Multiplexing on SMARC Edge

The i.MX 8M Plus SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8M Plus SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8M Plus SoC pin connections to the SMARC edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8M Plus Hardware Reference Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SMARC SOM Edge connector for iWave's BSP reusability and to have compatible SMARC modules in future for upgradability.

Table 7: i.MX 8M Plus SoC IOMUX for SMARC Edge Connector interfaces

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
MIPI CSI0	S9	E22	MIPI_CSI1_CLK_N							MIPI_CSI1_CLK_N
	S8	D22	MIPI_CSI1_CLK_P							MIPI_CSI1_CLK_P
	S12	E18	MIPI_CSI1_D0_N							MIPI_CSI1_D0_N
	S11	D18	MIPI_CSI1_D0_P							MIPI_CSI1_D0_P
	S15	E20	MIPI_CSI1_D1_N							MIPI_CSI1_D1_N
	S14	D20	MIPI_CSI1_D1_P							MIPI_CSI1_D1_P
	S6	AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	GPIO5_IO12		CCM_CLKO1
	S5	AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18		I2C3_SCL
	S7	AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19		I2C3_SDA
MIPI CSI1	P4	B23	MIPI_CSI2_CLK_N							MIPI_CSI2_CLK_N

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
	P3	A23	MIPI_CSI2_CLK_P							MIPI_CSI2_CLK_P
	P8	B25	MIPI_CSI2_D0_N							MIPI_CSI2_D0_N
	P7	A25	MIPI_CSI2_D0_P							MIPI_CSI2_D0_P
	P11	B24	MIPI_CSI2_D1_N							MIPI_CSI2_D1_N
	P10	A24	MIPI_CSI2_D1_P							MIPI_CSI2_D1_P
	P14	B22	MIPI_CSI2_D2_N							MIPI_CSI2_D2_N
	P13	A22	MIPI_CSI2_D2_P							MIPI_CSI2_D2_P
	P17	B21	MIPI_CSI2_D3_N							MIPI_CSI2_D3_N
	P16	A21	MIPI_CSI2_D3_P							MIPI_CSI2_D3_P
	S1	AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO3		I2C5_SCL
	S2	AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO4		I2C5_SDA
MIPI DSI0	S135	B18	MIPI_DSI1_CLK_N							MIPI_DSI1_CLK_N
	S134	A18	MIPI_DSI1_CLK_P							MIPI_DSI1_CLK_P
	S126	B16	MIPI_DSI1_D0_N							MIPI_DSI1_D0_N
	S125	A16	MIPI_DSI1_D0_P							MIPI_DSI1_D0_P
	S129	B17	MIPI_DSI1_D1_N							MIPI_DSI1_D1_N

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
	S128	A17	MIPI_DSI1_D1_P							MIPI_DSI1_D1_P
	S132	B19	MIPI_DSI1_D2_N							MIPI_DSI1_D2_N
	S131	A19	MIPI_DSI1_D2_P							MIPI_DSI1_D2_P
	S138	B20	MIPI_DSI1_D3_N							MIPI_DSI1_D3_N
	S137	A20	MIPI_DSI1_D3_P							MIPI_DSI1_D3_P
	S139	AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO3		I2C5_SCL
	S140	AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO4		I2C5_SDA
	S141	AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21		PWM1_OUT
	S127	L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_0	UART4_TX	GPIO3_IO7	CORESIGHT_TRACE05	GPIO3_IO7
	S133	L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B		GPIO3_IO8	CORESIGHT_TRACE06	GPIO3_IO8
LVDS1	S109	B28	LVDS1_CLK_N							LVDS1_CLK_N
	S108	A28	LVDS1_CLK_P							LVDS1_CLK_P
	S112	B26	LVDS1_D0_N							LVDS1_D0_N
	S111	A26	LVDS1_D0_P							LVDS1_D0_P
	S115	B27	LVDS1_D1_N							LVDS1_D1_N
	S114	A27	LVDS1_D1_P							LVDS1_D1_P
	S118	C28	LVDS1_D2_N							LVDS1_D2_N
	S117	B29	LVDS1_D2_P							LVDS1_D2_P
	S121	D28	LVDS1_D3_N							LVDS1_D3_N
	S120	C29	LVDS1_D3_P							LVDS1_D3_P
	S122	AE16	SAI5_RX_DATA0	SAI1_TX_DATA2	PWM2_OUT	I2C5_SCL	PDM_BIT_STREAM0	GPIO3_IO21		PWM2_OUT
	S107	R26	NAND_DQS	QSPI_A_DQS	SAI3_MCLK	ISP_SHUTTER_OPEN_0		GPIO3_IO14		GPIO3_IO14

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
	S116	AD22	HDMI_CEC			I2C6_SCL	FLEXCAN2_TX	GPIO3_IO28		GPIO3_IO28
HDMI	P102	AJ24	HDMI_TXC_N							HDMI_TXC_N
	P101	AH24	HDMI_TXC_P							HDMI_TXC_P
	P99	AJ25	HDMI_TX0_N							HDMI_TX0_N
	P98	AH25	HDMI_TX0_P							HDMI_TX0_P
	P96	AJ26	HDMI_TX1_N							HDMI_TX1_N
	P95	AH26	HDMI_TX1_P							HDMI_TX1_P
	P93	AJ27	HDMI_TX2_N							HDMI_TX2_N
	P92	AH27	HDMI_TX2_P							HDMI_TX2_P
	P104	AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	FLEXCAN2_RX	GPIO3_IO29		HDMI_HPD
	P105	AC22	HDMI_SCL			I2C5_SCL	FLEXCAN1_TX	GPIO3_IO26		HDMI_SCL
	P106	AF22	HDMI_SDA			I2C5_SDA	FLEXCAN1_RX	GPIO3_IO27		HDMI_SDA
SD Interface	P36	AB29	USDHC2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13		USDHC2_CLK
	P34	AB28	USDHC2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14		USDHC2_CMD
	P39	AC28	USDHC2_DATA0		I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO15		USDHC2_DATA0
	P40	AC29	USDHC2_DATA1		I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO16		USDHC2_DATA1
	P41	AA26	USDHC2_DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO17		USDHC2_DATA2
	P42	AA25	USDHC2_DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO18	SRC_EARLY_RESET	USDHC2_DATA3
	P37	AD28	USDHC2_RESET_B					GPIO2_IO19	SRC_SYSTEM_RESET	GPIO2_IO19
	P33	AC26	USDHC2_WP					GPIO2_IO20	CORESIGHT_EVENTI	GPIO2_IO20
	P35	AD29	USDHC2_CD_B					GPIO2_IO12		USDHC2_CD_B

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
SPI1	P54	AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13		ECSPI2_SS0
	P56	AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10		ECSPI2_SCLK
	P57	AF8	I2C4_SCL	PWM2_OUT	PCIE_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20		ECSPI2_MISO
	P58	AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11		ECSPI2_MOSI
SPI0	P43	AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC		GPIO5_IO9		ECSPI1_SS0
	P44	AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RX_SYNC		GPIO5_IO6		ECSPI1_SCLK
	P45	AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RX_DATA0		GPIO5_IO8		ECSPI1_MISO
	P46	AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RX_BCLK		GPIO5_IO7		ECSPI1_MOSI
USB OTG1	P74	A6	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT		GPIO1_IO13
	S68	D10	USB1_D_P							USB1_D_P
	S69	E10	USB1_D_N							USB1_D_N
	S62	A10	USB1_TX_P							USB1_TX_P
	S63	B10	USB1_TX_N							USB1_TX_N
	S65	A9	USB1_RX_P							USB1_RX_P
	S66	B9	USB1_RX_N							USB1_RX_N
PCIe	P89	A15	PCIE_TXN_P							PCIE_TXN_P
	P90	B15	PCIE_TXN_N							PCIE_TXN_N
	P86	A14	PCIE_RXN_P							PCIE_RXN_P
	P87	B14	PCIE_RXN_N							PCIE_RXN_N
	S146	A4	GPIO1_IO14	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1	GPIO1_IO14
	P75	A5	GPIO1_IO12	USB1_OTG_PWR				SDMA2_EXT_EVENT[1]		GPIO1_IO12

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
UART2	P130	AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24		UART2_RX
	P129	AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25		UART2_TX
	P132	AF18	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0		UART2_RTS_B	GPIO4_IO30	PDM_BIT_STREAM1	UART2_RTS_B
	P131	AJ18	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK	UART2_CTS_B
UART1 (optional)	P136	AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23		UART1_TX
	P137	AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22		UART1_RX
	P138	AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	CAN2_TX	GPIO5_IO26		UART1_CTS_B
	P139	AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	CAN2_RX	GPIO5_IO27		UART1_RTS_B
UART3	P135	N25	NAND_ALE	QSPI_A_SCLK	SAI3_TX_BCLK	ISP_FL_TRIG_0	UART3_RX	GPIO3_IO0	CORESIGHT_TRACE_CLK	UART3_RX
	P134	L26	NAND_CE0_B	QSPI_A_SS0_B	SAI3_TX_DATA0	ISP_SHUTTER_TRIG_0	UART3_TX	GPIO3_IO1	CORESIGHT_TRACE_CTL	UART3_TX
UART4	P141	AJ5	UART4_RX	UART2_CTS_B	PCIE_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28		UART4_RX
	P140	AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29		UART4_TX
Audio SAI0	S51	AH18	SAI3_TX_DATA0	SAI2_TX_DATA3	SAI5_RX_DATA3	GPT1_CAPTURE2	SPDIF1_EXT_CLK	GPIO5_IO1		SAI3_TX_DATA0
	S52	R25	NAND_DATA00	QSPI_A_DATA0	SAI3_RX_DATA0	ISP_FLASH_TRIG_0	UART4_RX	GPIO3_IO6	CORESIGHT_TRACE04	SAI3_RX_DATA0
	S53	AH19	SAI3_TX_BCLK	SAI2_TX_DATA2	SAI5_RX_DATA2	GPT1_CAPTURE1	UART2_TX	GPIO5_IO0	PDM_BIT_STREAM2	SAI3_TX_BCLK
	S50	AC16	SAI3_TX_SYNC	SAI2_TX_DATA1	SAI5_RX_DATA1	SAI3_TX_DATA1	UART2_RX	GPIO4_IO31	PDM_BIT_STREAM3	SAI3_TX_SYNC

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
Audio SAI1	S41	AJ14	SAI2_RX_DATA0	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_OUT	SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO23	PDM_BIT_STREAM3	SAI2_RX_DATA0
	S42	AH15	SAI2_TX_BCLK	SAI5_TX_DATA2		FLEXCAN1_RX		GPIO4_IO25	PDM_BIT_STREAM1	SAI2_TX_BCLK
	S40	AH16	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26		SAI2_TX_DATA0
	S39	AJ17	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2	SAI2_TX_SYNC
	S38	AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_AUX_IN	GPIO4_IO27	SAI3_MCLK	SAI2_MCLK
CAN	P143	AD16	SAI5_RX_DATA1	SAI1_TX_DATA3	SAI1_TX_SYNC	SAI5_TX_SYNC	PDM_BIT_STREAM1	GPIO3_IO22	FLEXCAN1_TX	FLEXCAN1_TX
	P144	AF16	SAI5_RX_DATA2	SAI1_TX_DATA4	SAI1_TX_SYNC	SAI5_TX_BCLK	PDM_BIT_STREAM2	GPIO3_IO23	FLEXCAN1_RX	FLEXCAN1_RX
	P145	AE14	SAI5_RX_DATA3	SAI1_TX_DATA5	SAI1_TX_SYNC	SAI5_TX_DATA0	PDM_BIT_STREAM3	GPIO3_IO24	FLEXCAN2_TX	FLEXCAN2_TX
	P146	AF14	SAI5_MCLK	SAI1_TX_BCLK	PWM1_OUT	I2C5_SDA		GPIO3_IO25	FLEXCAN2_RX	FLEXCAN2_RX
GPIO	P108	AC12	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		ENET1_RX_ER	GPIO4_IO18		GPIO4_IO18
	P109	AJ13	SAI1_TX_DATA7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19		GPIO4_IO19
	P110	AJ9	SAI1_RX_SYNC				ENET1_1588_EVENT0_IN	GPIO4_IO0		GPIO4_IO0
	P111	AH8	SAI1_RX_BCLK			PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO1		GPIO4_IO1
	P112	AC10	SAI1_RX_DATA0		SAI1_TX_DATA1	PDM_BIT_STREAM0	ENET1_1588_EVENT1_IN	GPIO4_IO2		GPIO4_IO2

Interface/ Function	SMARC Edge Pin Number	i.MX 8M Plus SoC Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default
	P113	AD14	SAI5_RX_BCLK	SAI1_TX_DATA1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20		GPIO3_IO20
	P114	AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1	GPIO4_IO22
	P115	AH17	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM2	GPIO4_IO21
	P116	AJ19	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI5_RX_SYNC	SAI3_RX_DATA1	SPDIF1_IN	GPIO4_IO28	PDM_BIT_STREAM0	GPIO4_IO28
	P117	AF10	SAI1_RX_DATA1			PDM_BIT_STREAM1	ENET1_1588_EVENT1_OUT	GPIO4_IO3		GPIO4_IO3
	P118	AC14	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL		GPIO3_IO19		GPIO3_IO19
	P119	AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO5		GPIO5_IO5
I2C	S48	AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_AUX_IN	GPIO5_IO16		I2C2_SCL
	S49	AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17		I2C2_SDA
Control Signal	P126	B8	GPIO1_IO9	ENET_QOS_1588_EVENT0_OUTPWM2_OUT	PWM2_OUT	ISP_SHUTTER_OPEN_1	USDHC3_RESET_B	SDMA2_EXT_EVENT[0]		GPIO1_IO9
	S145	B6	GPIO1_IO2	WDOG1_WDOG_B		ISP_FLASH_TRIG_0		WDOG1_WDOG_ANY		WDOG1_WDOG_B

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Plus SMARC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VDD_IN that may vary over the 4.5V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.5V to 5.25V. Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX 8M Plus SMARC SOM.

Table 8: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VDD_IN [1]	4.5V[1]	5V	5.25V	±50mV
2	VDD_RTC [2]	2.8V	3V	3.3V	±20mV

[1] i.MX 8M Plus SMARC SOM is designed to work with VDD_IN input power rail from SMARC PCB Edge connector only. VDD_IN can be as low as 3.3V with sufficient current if fan is not used.

[2] i.MX 8M Plus SMARC SOM use this voltage as backup power source to RTC controller when VDD_IN is off.

3.1.2 Power Input Sequencing

The i.MX 8M Plus SMARC SOM's Power Input sequence requirement is explained below.

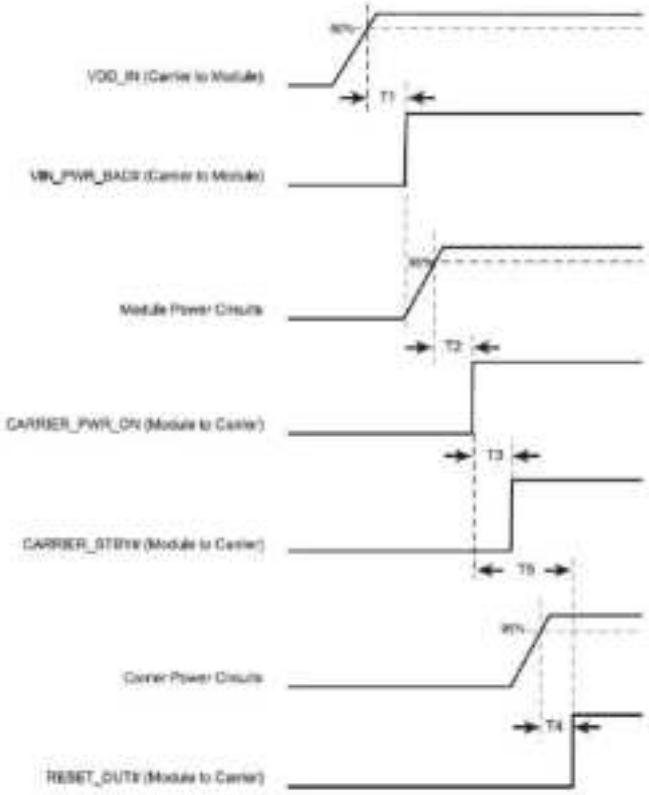


Figure 7: Power Input Sequencing

Table 9: Power Sequence Timing

Item	Description	Value
T1	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T2	VIN_PWR_BAD# rise time to SOM Power rise time	≥ 0 ms
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	≥ 0 ms
T4	Carrier power circuits are up to RESET_OUT# rise	≥ 0 ms
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 to 500ms

3.1.3 Power Consumption

Table 10: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Power Consumption During Booting		
During Booting	VDD_IN	0.509A/2.435W
Run Mode Power Consumption[1]		
Play Video run in MIPI display (Gstreamer)	VDD_IN	0.47A/2.35W
Camera Streaming in HDMI display	VDD_IN	0.417A/2.085
Play 1080p Video run in 4K HDMI display (Gstreamer)	VDD_IN	0.487A/2.435W
Play Audio	VDD_IN	0.316A/1.58W
Ping Bluetooth	VDD_IN	0.319A/1.595W
Ping Wi-Fi	VDD_IN	0.365A/1.825W
Ping Ethernet (Eth0 and Eth1)	VDD_IN	0.506A/2.53W
eMMC to Standard SD file transfer	VDD_IN	0.424A/2.12W
eMMC to USB3.0 file transfer	VDD_IN	0.442A/2.21W
eMMC to USB2.0 file transfer	VDD_IN	0.494A/2.47W
eMMC to M.2 PCIe file transfer	VDD_IN	0.514A/2.57W
Bluetooth file transfer	VDD_IN	0.414A/2.07W
Wi-Fi file transfer	VDD_IN	0.667A/3.335W
Ethernet Streaming (Video Play)	VDD_IN	0.684A/3.42W
GPU Processor -Graphics 3D Test	VDD_IN	0.532A/2.66W
Dhrystone	VDD_IN	0.42A/2.1W
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in MIPI display, 10.1 inch LVDS & HDMI • Camera Streaming • Ethernet (eth0 & eth1) Run the ping (65500 packet size) • Wi-Fi- Run the ping teston back ground • FileTransfer - Transfer the 1GB files in storage devices • Run the dry2 application on back ground • GPU Processor -Graphics 3D Test	VDD_IN	1.163A/5.815W
Low Power Mode Power Consumption		
System Idle Mode.	VDD_IN	0.25A/1.25W
Deep Sleep Mode.	VDD_IN	0.032A/0.16W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	0.0003A/0.0009W

[1] *Power consumption measurements are done in iWave 's i.MX 8M Plus SoC based SMARC Development platform with iWave's iW-PRGQZ-SC-01-R2.0-REL1.0-Linux5.15.71 BSP.*

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Plus SMARC SOM.

Table 11: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2,3]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]The LBEE5HY1MW Wi-Fi & BT module supports operating temperature -30°C to 85°C with the default module's firmware. To set the module temperature to industrial grade in firmware, please contact iWave.

[3] For more information on Thermal solution & Heat sink/ Heat Spreader refer the following section.

3.2.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to SoC via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

Note: iWave supports Heat Sink/ Heat Spreader Solution for i.MX 8M Plus SMARC SOM. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

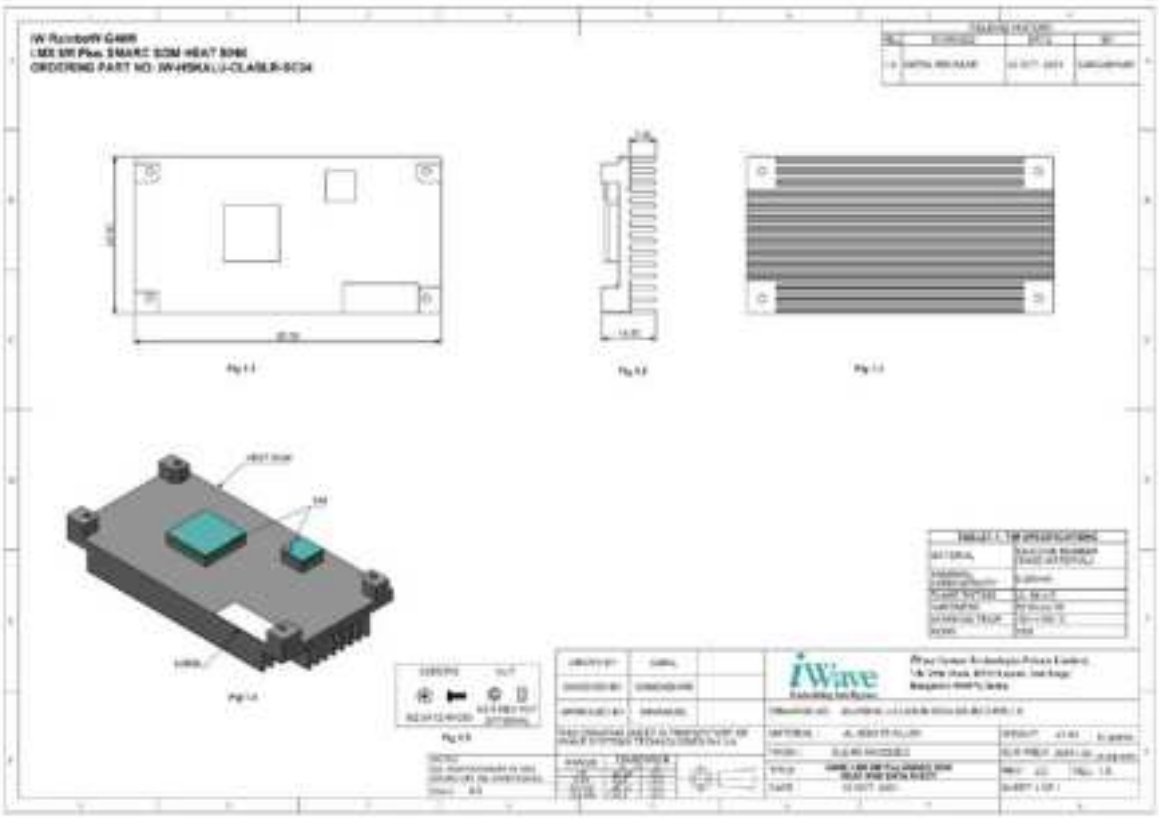


Figure 8: i.MX 8M Plus SMARC SOM Heat Sink Mechanical Dimensions

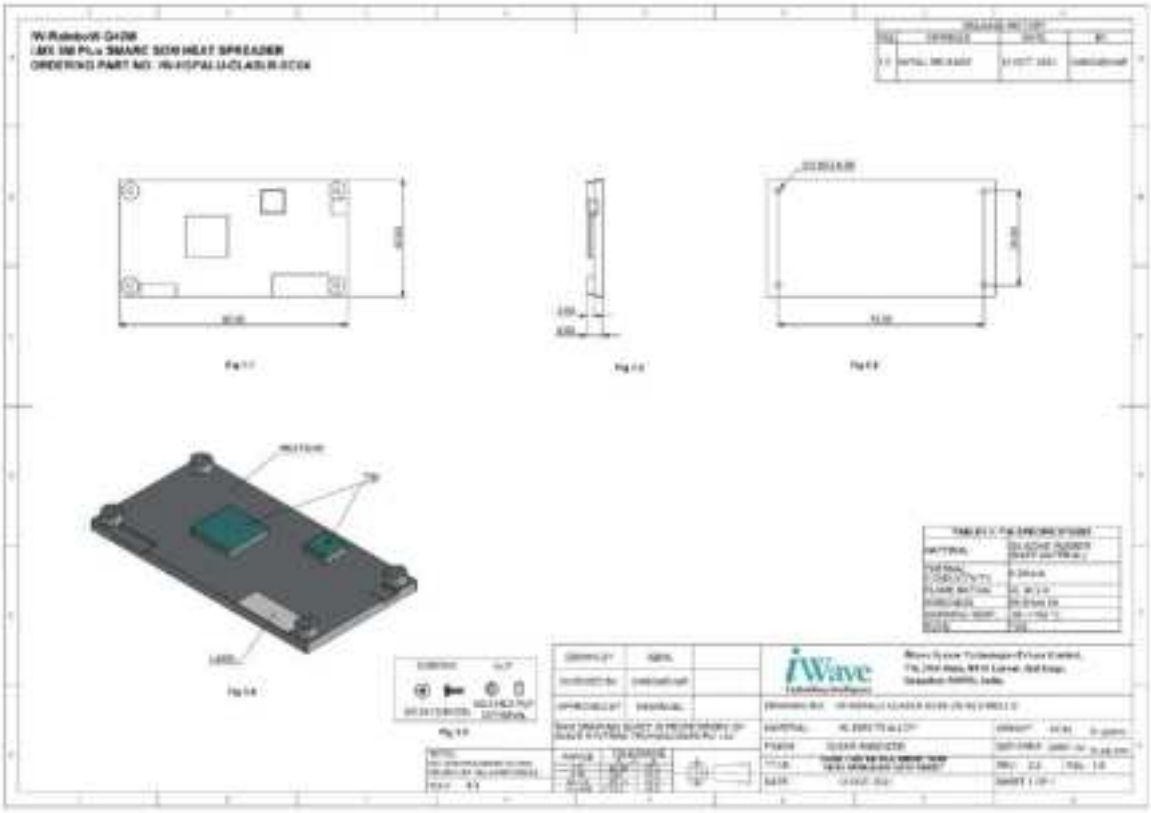


Figure 9: i.MX 8M Plus SMARC SOM Heat Spreader Mechanical Dimensions

3.2.3 RoHS Compliance

iWave's i.MX 8M Plus SMARC SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 8M Plus SMARC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 8M Plus SMARC SOM Mechanical Dimensions

i.MX 8M Plus SMARC SOM PCB size is 50 mm x 82mm x 1.2mm. The i.MX 8M Plus SMARC SOM PCB thickness is 1.2mm±0.15mm, top side maximum height component is 3.5mm (debug Connector) which is optional in default configuration hence 3.4mm FAN header will be the maximum height on Top side in default configuration followed by optional GNSS module (2.6mm) & RTC Controller (1.75mm). In bottom side maximum height component is optional MIPI CSI Camera connector (2mm) followed by D11 diode (1.35mm).

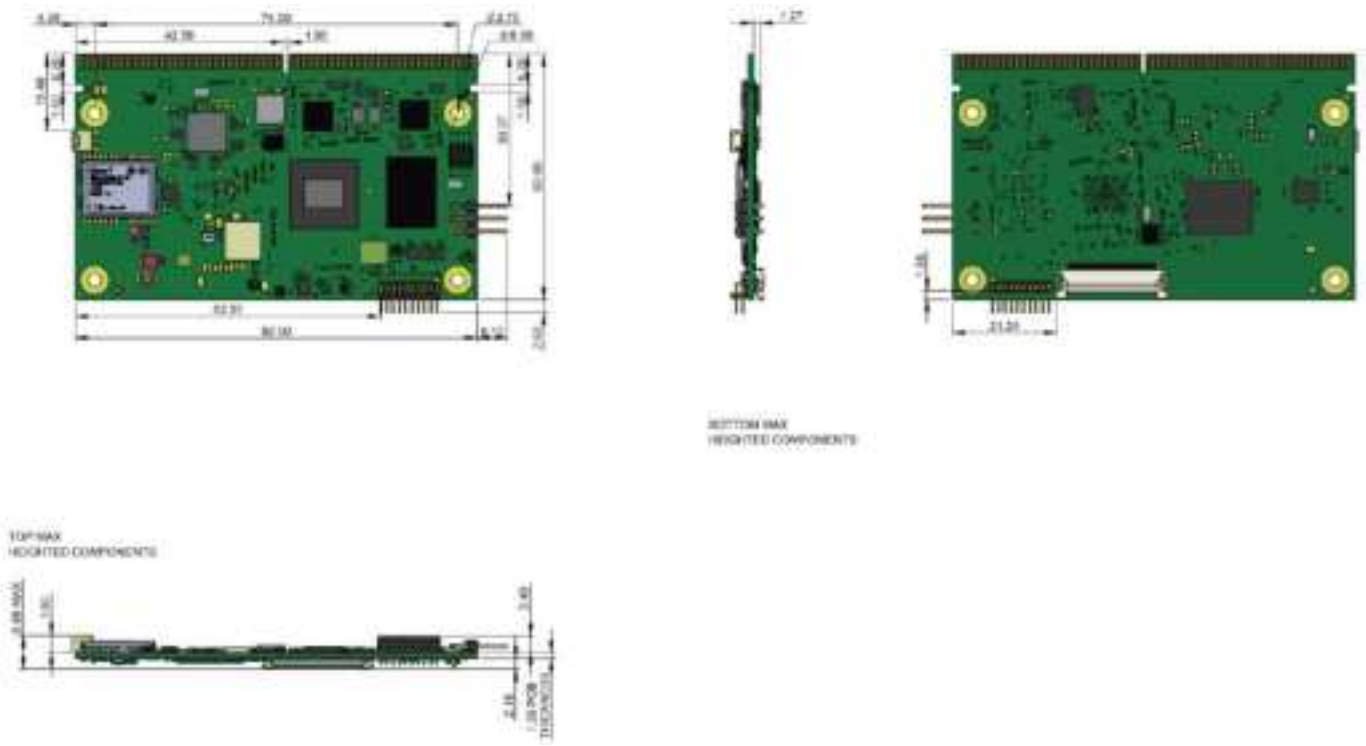


Figure 10: i.MX 8M Plus SMARC SOM Mechanical Dimensions

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8M Plus SMARC SOM variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 12: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G40M - i.MX 8M Plus SMARC SOM (Industrial grade) With Wi-Fi & 2 x Ethernet		
iW-G40M-SCPQ-4L001G-E008G-BIA	i.MX 8M Plus Quad, 1GB LPDDR4, 8GB eMMC, 2xEthernet - With Wi-Fi, BT	-40°C to 85°C
iW-G40M-SCPQ-4L002G-E016G-BIA	i.MX 8M Plus Quad, 2GB LPDDR4, 16GB eMMC, 2xEthernet - With Wi-Fi, BT	-40°C to 85°C
iW-G40M-SCPQ-4L004G-E016G-BIA	i.MX 8M Plus Quad, 4GB LPDDR4, 16GB eMMC, 2xEthernet - With Wi-Fi, BT	-40°C to 85°C

Note: Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.

5. APPENDIX

5.1 i.MX 8M Plus SMARC SOM Development Platform

iWave Systems supports iW-RainboW-G40D-i.MX 8M Plus SMARC SOM Development Platform which is targeted for quick validation of i.MX 8M Plus SoC based SMARC SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete SMARC supported features.

For more details on i.MX 8M Plus SMARC SOM and Development Platform, visit the below web link.

https://www.iwavesystems.com/product/i-mx-8m-plus-smarc-som/

Figure 11: i.MX 8M Plus SMARC SOM Development Platform

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