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FPGA IP CORE

iW- VME Slave IP

The ANSI/VITA 1.0-1994 or VME64 specification establishes a framework for 8-, 16-, and 32-bit parallel bus computer architectures that can implement single and multiprocessor systems. The VMEbus specification defines an interfacing system used to interconnect microprocessors, data storage, and peripheral control devices in a closely coupled hardware configuration.

iWave's IP is compliant to ANSI/VITA1.0-1994 and implements the slave configuration of VMEbus data transfer layer consisting of the Data Transfer Bus and the Priority Interrupt Bus modules. This IP can be considered as a VME to AXI bus bridge and can be implemented in any FPGA having interface to a VME Bus Interface.

Highlights

- Core is compliant to ANSI/VITA 1.0-1994
- VME Slave IP provides a bus bridge between VME and AXI interfaces
- Supports A32, A16 and A8 addressing modes with D16 data

Features

- Compliant with ANSI/VITA 1.0-1994 VME64 Bus Standard
- VME to AXI Bus Bridge
- VME bus Module Type
  - Slave with Priority Based Interrupts
- Board Address: Hardware Configurable up to 8 bits
- Data Format Supported
  - 16 bits
  - 8 bits
- Transfer Modes
  - Write
  - Read
  - Block Write
  - Block Read
- Address Modes
  - A32 Slave: 09, 0B, 0D and 0F (Data and Block Transfer)
  - A24 Slave: 39, 3B, 3D and 3F (Data and Block Transfer)
  - A16 Slave: 29 and 2D (Data Access, No Block Transfers)
- Block Transfer
  - Maximum 256 bytes
- User Interface
  - AXI-4 Lite

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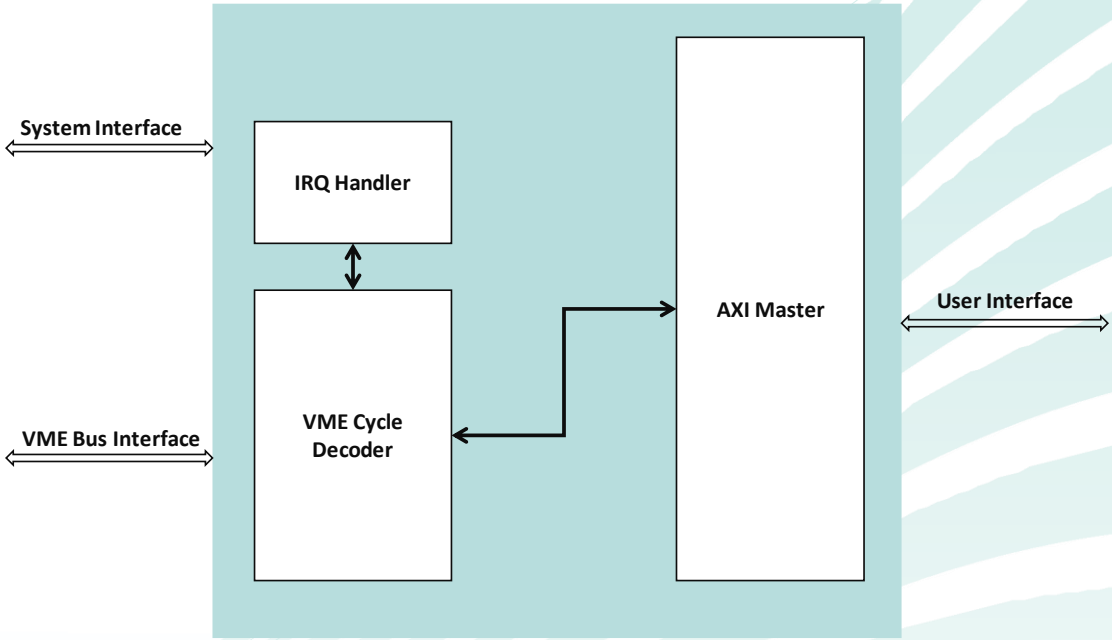
iW - VME Slave IP block diagram



VME Slave IP Core (VME to AXI Bridge)

Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site or Multi Site
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Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

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iW - VME Slave FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/vme-slave-ip-core-vme-to-axi-bridge/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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