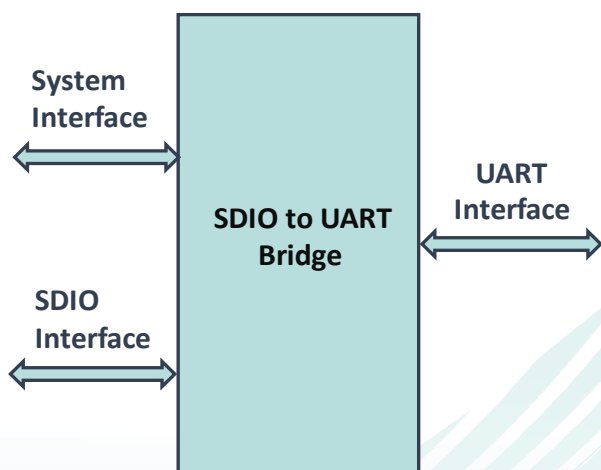


## iW SDIO 3.0 to UART Bridge IP



iW-SDIO to UART bridge is a IP core which converts SDIO slave to UART bus interface. SDIO Slave controller facilitates the design of SDIO cards and reduces the development time. By using this IP core, customers no longer need to spend time on handling the SD bus protocol since such function is provided by the core.

### Application

- Used as Bridge between SDIO interface and UART

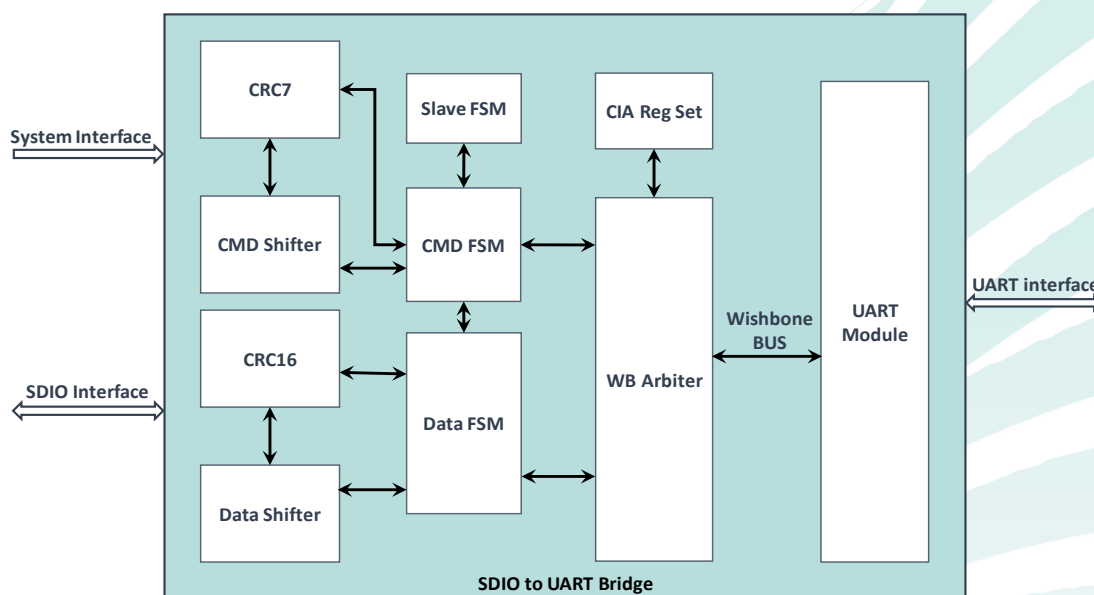
### Highlights

- SDIO interface supported by the bridging IP enables a low-cost and small size implementation

### Features

- Compliant with SD Physical Specification Version 3.00 and SDIO Specification Version 3.00.
- Supports SPI, 1-bit and 4bit SD modes.
- Supports SDIO Interrupt feature
- Supports all mandatory SDIO Commands/Response types
  - SPI Mode: CMD0, CMD5, CMD52, CMD53, CMD59
  - SD Mode: CMD0, CMD3, CMD5, CMD7, CMD52, CMD53.
- CRC7 checking/generation for Command/Response
- CRC16 checking/generation for Data transfer.
- Supports High Speed Mode (up to 50Mhz) of operation.
- Data Transfer in Multi Byte and Multi Block mode using CMD53.
- SDIO only implementation, Combo card features are not supported
- Optional Code Storage Area (CSA) is not supported
- Suspend/Resume Features not supported
- Supports UART16550 function
  - Programmable baud generator divides any input clock by 1 to (216 – 1) and generates the 16x clock.
  - MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1/2, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud)
  - Line break generation and detection
  - Independently controlled transmit, receive, line status, and data set interrupts

## iW SDIO to UART Bridge Block Diagram



## Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual
- Linux driver reference

## Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License – Single Site or Multi Site

## Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave Systems, a leading FPGA design house enhances your design productivity by providing an extensive suite of proven, optimized and easy-to-use FPGA IP Cores along with reference designs to complement and quicken your applications development. Our extensive suite of IP Cores covers all key markets and applications. Along with the rich set of FPGA IP cores, iWave offers custom FPGA designs tailored to meet the client specifications which includes RTL Design, Integration of iWave's or 3rd Party IP Cores on our FPGA SOMs with Carrier Card/ Custom Hardware/ Off-the-Shelf Evaluation Kits to provide end-to-end solutions targeting Low-Power, High-Performance and Optimized Designs

## iW – SDIO 3.0 to UART Bridge FPGA IP

The IP can be ordered online from the iWave Website <http://www.iwavesystems.com/product/sdio-to-uart-controller/>  
Or from our Local Partners in your region <http://www.iwavesystems.com/about-us/business-partner.html>

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