![iWave - Embedding Intelligence logo]
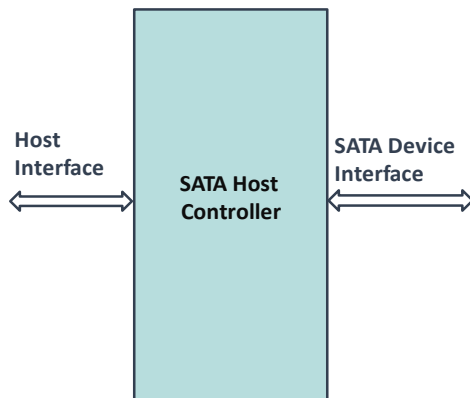
iWave's SATA Host Core is available for integration into host FPGA designs to provide an industry- compliant SATA 1.5-Gbps, SATA 3.0-Gbps and SATA 6.0-Gbps interface. Serial ATA (SATA) are computer bus standards that have the primary function of transferring data between the FPGA and mass storage devices such as hard disk. SATA host controller along with AHCI controller enables the software to communicate with the SATA drives which is best suited for SOC devices.

Applications

- Used in consumer, computer and storage applications

Highlights

- AHCI controller along with SATA host controller best suits for SOC devices and SATA controller without AHCI layer can be used with Non SOC FPGA devices

- Controller provides simple AXI streaming TX and RX interface for the communication with Application layer.

- Supports most of the primitives and FIS types defined in SATA specification

Features

- Phy layer consists of Transceiver available in the FPGA which convert the parallel data to serial

- Phy layer supports clock recovery from serial data, 8B/10B encoding and decoding, Byte ordering and word alignment and OOB signaling

- Link layer supports the frame transmission and reception

- Link layer supports frame formation by adding the envelope and frame decomposition by removing envelope from received data

- Link layer supports CRC generation and calculation as well as scrambling and descrambling

- Link layer supports host and device flow control

- Link layer supports primitives such as ALIGN, DMAT, EOF, HOLD, HOLDA, R_ERR, R_IP, R_OK, R_RDY, SOF, SYNC, WTRM, X_RDY

- Transport layer supports 32 bit AXI stream interface for Tx and RX towards user interface

- Transport layer supports formatting of the FISes and control information based on FIS type

- Transport layer reports frame transmission and reception as well as error status

- Transport layer supports FISes such as Register FIS, DMA Activate FIS, DMA Setup FIS, Data FIS, PIO Setup FIS, Set Device Bits FIS

iW- SATA Host Controller block diagram
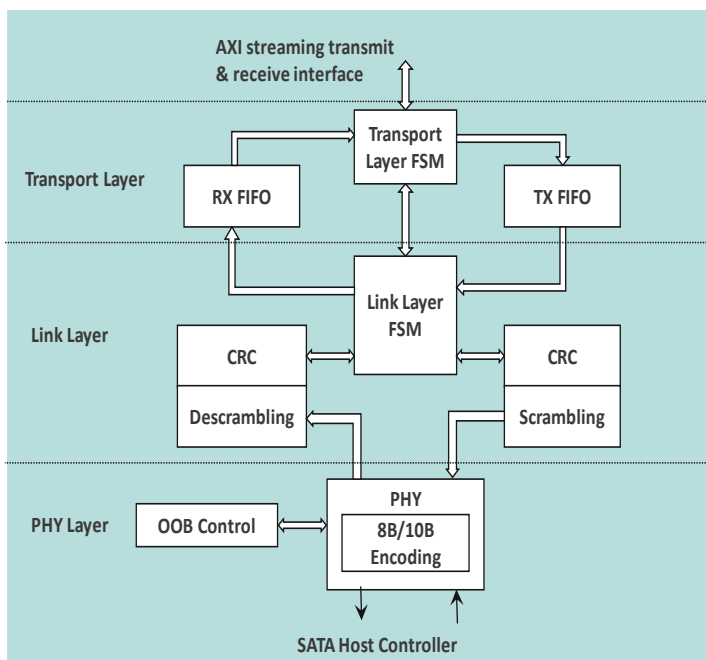
Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual
- Linux driver reference

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License – Single Site or Multi Site

Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave Systems, a leading FPGA design house enhances your design productivity by providing an extensive suite of proven, optimized and easy-to-use FPGA IP Cores along with reference designs to complement and quicken your applications development. Our extensive suite of IP Cores covers all key markets and applications. Along with the rich set of FPGA IP cores, iWave offers custom FPGA designs tailored to meet the client specifications which includes RTL Design, Integration of iWave's or 3rd Party IP Cores on our FPGA SOMs with Carrier Card/ Custom Hardware/ Off-the-Shelf Evaluation Kits to provide end-to-end solutions targeting Low-Power, High-Performance and Optimized Designs

iW SATA Host Controller FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/sata-host-controller/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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