![iWave - Embedding Intelligence logo]

iW - PCI Controller

PCI Interface

User Interface

PCI Controller provides an interface between the PCI bus and user interface. PCI core interface is processor independent, enabling an efficient transition to future processor generations and use with multiple processors.
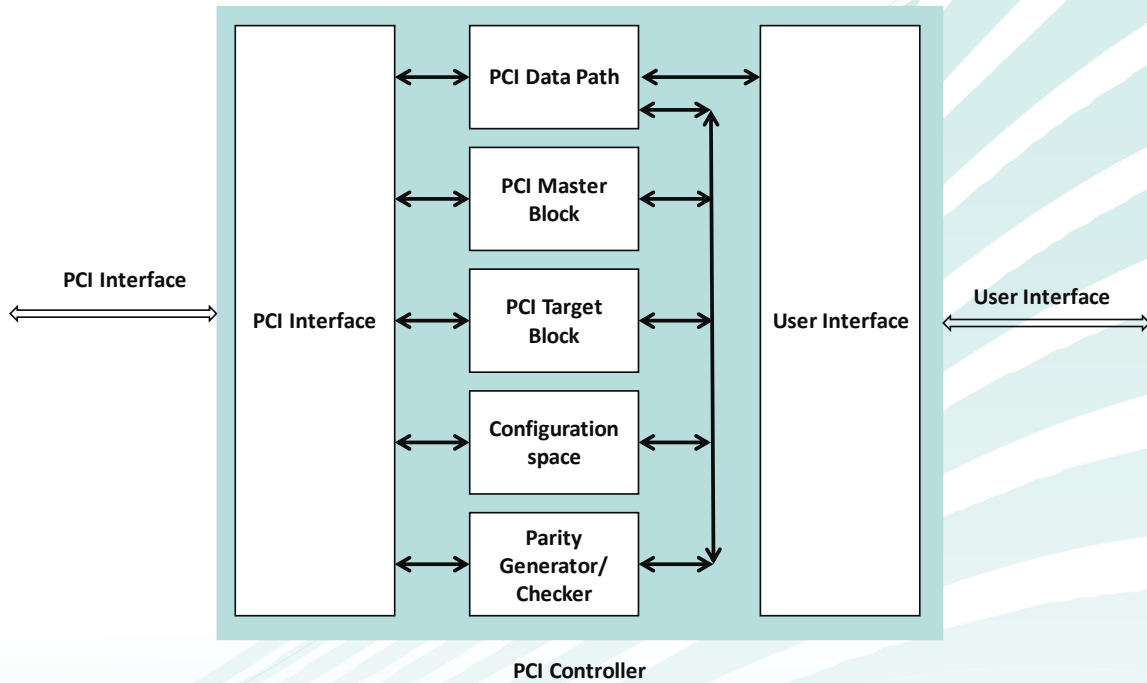
Highlights

- Compliant with PCI Specification 2.3

- Separate initiator and target functional blocks.

Features

- 64-bit, 33/66MHz PCI interface

- Supported initiator commands and functions:

  Parity generation, parity error detection

  - Configurations read / write

  - Memory read / write, memory read multiple, memory read line

  - I/O read / write

  - Interrupt acknowledge, special cycles

  - Parity generation, parity error detection

  - Master abort

- Supports a very generic user interface

  - Supported target commands and functions,

Type 0 configuration space header

  - Up to six base address registers.

  - Memory read / write, memory read multiple, memory read line

  - Target abort, target retry, target disconnect

  - I/O read / write

  - Medium speed DEVSEL timing

  - Interrupt acknowledge

- PCI Configuration base registers are configurable from header file

iW - PCI Controller IP block diagram

PCI Interface

PCI Interface

PCI Data Path

PCI Master Block

PCI Target Block

Configuration space

Parity Generator/ Checker

User Interface

User Interface

PCI Controller

Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License – Single Site or Multi Site

Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

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iW - PCI Controller FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/pci-controller/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html