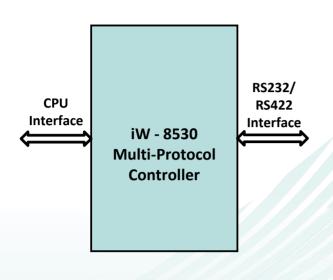




iW-8530 Multi-Protocol Controller IP



iW - 8530 MPSC Controller (Multi-Protocol Serial Communication Controller) is a general-purpose communication controller which consists of two sets of bi-directional parallel / serial converter circuits for data communication.

Highlights

- Compatible with uPD72001 and 85C30
- Controller supports all three serial protocols (UART, Mono-Sync, Bi-Sync, HDLC and SDLC)

Features

- Hardware features
 - Transmit buffer (2 Byte Depth)
 - o Receive buffer (4 Byte Depth)
 - Interrupt control function
 - DMA request: 2 for TX and 2 for Rx
 - o Overrun error detection
 - Baud rate generator
 - Self-loop back test function
 - o GPIO: 4 pins x 2
 - DPLL supported
- Communication protocol features
 - Start-stop synchronization
 - Character bit length: 5, 6, 7, 8
 - Stop bit length: 1, 1.5, 2
 - Clock rate: x1, x16, x32, x64
 - Parity generation, check
 - Framing error detection
 - Break generation, detection
 - Character oriented protocol (COP)
 - Operating mode: Mono-sync, Bi-sync, External sync
 - Character bit length: 5, 6, 7, 8
 - SYNC character bit length: 6, 8
 - Character synchronization: internal/external
 - Block check sequence (BCS) generation, check: CRC16, CRC-CCITT

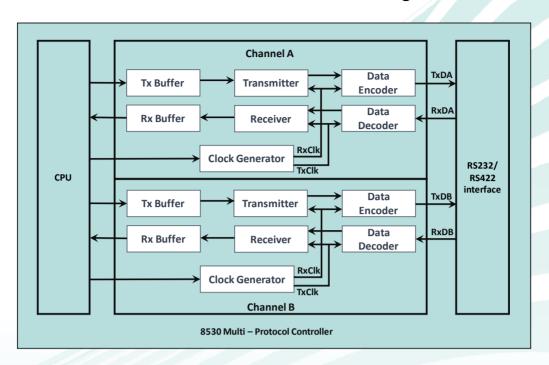
- Parity generation, check
- SYNC character automatic transmission, detection, rejection
- Bit oriented protocol (BOP)
 - Operation mode: HDLC (High-level Data Link Control), SDLC
 - (Synchronous Data Link Control), SDLC Loop
 - Flag transmission, detection
 - Zerinsertion, rejection
 - Address field detection (1 byte)
 - FCS (Frame Check Sequence) generation, detection
 - Short frame detection
 - Abort automatic transmission, detection
 - Idle detection
 - GAhead detection
 - Transmit number data control

Processing data format

- Encode/decode of NRZ (Non-Return to Zero)
- Encode/decode of NRZI (Non-Return to ZerInverted)
- Encode/decode of FM (Frequency Modulation)
- Decode in Manchester mode



iW 8530 Multi - Protocol IP block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License Single Site or Multi Site

Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave Systems, a leading FPGA design house enhances your design productivity by providing an extensive suite of proven, optimized and easy-to-use FPGA IP Cores along with reference designs to complement and quicken your applications development. Our extensive suite of IP Cores covers all key markets and applications. Along with the rich set of FPGA IP cores, iWave offers custom FPGA designs tailored to meet the client specifications which includes RTL Design, Integration of iWave's or 3rd Party IP Cores on our FPGA SOMs with Carrier Card/ Custom Hardware/ Off-the-Shelf Evaluation Kits to provide end-to-end solutions targeting Low-Power, High-Performance and Optimized Designs

iW-8530 Multi-Protocol FPGA IP

The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/8530-multi-protocol-controller Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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