iWave
Embedding Intelligence

FPGA IP CORE

iW- 80188EB Processor IP

The 80188EB is a powerful 16-bit microprocessor core, executes instruction list compatible with 80188EB microprocessor. The 80188EB core has a broad set of integrated peripherals, which helps reduce system development time and cost and is compatible with wide range of compilers and debuggers. The design along with multiple peripherals can be fit into single FPGA.

Highlights

- Compatible with 8237 and uPD71071
- The controller can improve the system performance by allowing external devices to transfer data directly to or from system memory
- Multi-mode programmability allows the user to select from three different transfer modes

Features

- **iW-80188EB CPU Core**
  - Multiplexed 20-bit address and 8-bit data bus
  - 1M-byte memory space divided into 4 segments
  - 64K-byte IO space
  - Non Maskable Interrupt support
  - Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16 x 16-bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)
- **CPU On-Chip Peripherals**
  - Programmable Timer / Counter Unit
    - Three programmable independent 16-bit timers
    - TOUT0 to TOUT1 pin outputs
    - TIN0 & TIN1 used either as clock or control signals
    - Timer-2 can be used to clock other two timers
    - Internal / external input clock selectable
  - Serial Communications Unit
    - RS-232-C protocol support (on-chip CTS_N, SINT_N pins)
    - Both synchronous and asynchronous modes are supported
    - Two independent identical channels
    - Full duplex operation in asynchronous mode
    - Half-duplex operation in synchronous mode
    - Programmable seven, eight or nine data bits in asynchronous mode
    - Independent baud rate generator
    - Double-buffered transmit and receive
    - Clear-to-Send feature for transmission
    - Break character transmission and detection
    - Programmable even, odd or no parity
    - Detects both framing and overrun errors
    - Supports interrupt on transmit and receive
  - Interrupt Controller Unit
    - Edge trigger / level trigger selectable
    - Individually maskable interrupt requests
    - Programmable interrupt request priority orders
    - Supports Cascading (Only INTP0 and INTP1) and polling mode
    - 5 external interrupt request inputs (INTP0 to INTP4)
    - 2 internal interrupt input pins (SCU and TCU)
  - Chip Select Unit
    - Ten programmable chip-select outputs
    - Programmable start and stop addresses
    - Memory or I/O bus cycle decoder
    - Programmable wait-state generator
    - Provision to disable a chip-select
    - Provision to override bus ready
  - Clock Generator
  - Two 8-bit multiplexed Input/output Ports

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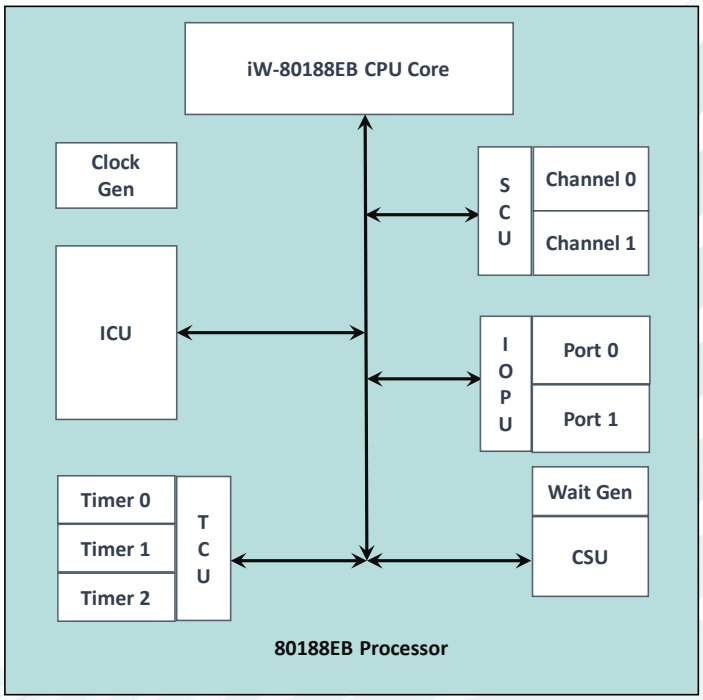
iW 80188EB Processor IP block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
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Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
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iW- 80188EB Processor FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/80188eb-processor/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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