# **FPGA IP CORE**



## iW-80186XL Processor IP

The 80186XL is a powerful 16-bit microprocessor core, executes instruction list compatible with 80186XL microprocessor. The 80186XL core has a broad set of integrated peripherals, which helps reduce system development time and cost and is compatible with wide range of compilers and debuggers. The design along with multiple peripherals can be fit into single FPGA..

## Highlights

- Quick migration of 80186XL based designs to an FPGA platform
- Replacement for 80186XL processor and ASICs

#### Features

- 80186XL CPU Core
  - Multiplexed 20-bit address and 16-bit data bus
  - 1MB memory space divided into 4 segments
  - 64K-byte IO space
  - Non Maskable Interrupt support
  - Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16x16 bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)
- CPU On-Chip Peripherals
- Programmable Timer / Counter Unit
  - Three programmable independent 16-bit timers
  - Internal / external input clock selectable
- o Direct Memory Access Unit
  - Two independent high-speed DMA channels
  - Data can be transferred between any combination of memory & IO space
  - DMA transfer can be initiated by external, internal request or by direct programming

- Both byte & word transfer is possible in case of 80186XL
- Interrupt Control Unit
  - Four external interrupt request inputs (INT0 to INT3).
  - Timer0, Timer1, Timer2 and DMA0, DMA1
    Interrupts (Internal Interrupts)
  - Edge or level triggered interrupt request inputs
  - Cascade with external 8259A interrupts (only on INT0 and INT1) operates in either Master mode or Slave mode
- Special fully nested mode support
- Chip Select Unit
  - Thirteen programmable chip-select outputs
  - Six of the chip-selects map only into memory address space, while the remaining seven can map into either memory or I/O address space
  - Memory or I/O bus cycle decoder
  - Programmable wait-state generator
- Clock Generator

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## iW - 80186XL Processor IP block diagram



#### **Deliverables**

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

#### **Licensing Options**

- Non-Transferable: Single Project/Product Netlist License Single Site or Multi Site ٠
- Non-Transferable: Multi Project /Product Netlist License Single Site or Multi Site ٠
- Non-Transferable: Single Project/Product RTL Source Code License Single Site or Multi Site
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### **Technical Support**

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

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#### iW-80186XL Processor FPGA IP

The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/80186xl-processor/ Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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