iWave
Embedding Intelligence

FPGA IP CORE

iW- 80186EC Processor IP

The 80186EC is a powerful 16-bit microprocessor core, executes instruction list compatible with 80186EC microprocessor. The 80186EC core has a broad set of integrated peripherals, which helps reduce system development time and cost and is compatible with wide range of compilers and debuggers. The design along with multiple peripherals can be fit into single FPGA.

Features

- **iW-80186EC CPU Core**
  - ❖ Multiplexed 20-bit address and 16-bit data bus
  - ❖ 1M-byte memory space divided into 4 segments
  - ❖ 64K-byte IO space
  - ❖ Non Maskable Interrupt support
  - ❖ Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16 x 16-bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)

- **CPU On-Chip Peripherals**
  - ❖ Programmable Timer / Counter Unit
    - Three programmable independent 16-bit timers
    - TOUT0 tTOUT1 pin outputs
    - TIN0 & TIN1 used either as clock or control signals
    - Timer-2 can be used to clock other two timers
    - Internal / external input clock selectable
  - ❖ Serial Communications Unit
    - RS-232-C protocol support(on-chip CTS_N, SINT_N pins)
    - Only asynchronous mode is supported
    - Two independent identical channels
    - Full duplex operation in asynchronous mode
    - Programmable seven, eight or nine data bits in asynchronous mode
    - Independent baud rate generator
    - Double-buffered transmit and receive
    - Clear-to-Send feature for transmission
    - Break character transmission and detection
    - Programmable even, odd or no parity
    - Detects both framing and overrun errors
    - Supports interrupt on transmit and receive
  - ❖ Interrupt Controller Unit
    - Edge trigger / level trigger selectable
    - Individually maskable interrupt requests
    - Programmable interrupt request priority orders
    - Supports Cascading and polling mode
    - 8 external interrupt request inputs (INTx ; x=0,1,2,..,7)
    - 7 internal interrupt input pins (SCU, TCU, and DMAU)
  - ❖ Chip Select Unit
    - Ten programmable chip-select outputs
    - Programmable start and stop addresses
    - Memory or I/bus cycle decoder
    - Programmable wait-state generator
    - Provision to disable a chip-select
    - Provision to override bus ready
  - ❖ Direct Memory Access Unit
    - Four DMA channels can be accessed independently
    - Priority of channels can be modified using priority registers.
    - DMA requests can be masked by DMA HALT registers.
    - Four separate External DMA requests pins.
    - Internal requests either by timer.
    - programmable software request to start the DMA.
    - The four channel DMAs are integrated using two channel module.
  - ❖ Watchdog Timer Unit
    - 32-bit down counter used,
    - Reload and disable option for the watchdog timer.
    - Asserts a signal to indicate if the program hangs, or some infinite loop occurs.
  - ❖ Multiplexed general purpose Input Output port
    - Three ports of total having 22 pins
    - A 8 pin inout port multiplexed with the Serial controller unit
    - A 8 pin output port multiplexed with Chip Select Unit.
    - A 6 pin output port multiplexed with DMA and SCU interrupts (4 pins) and two pins as general purpose inouts.
  - ❖ Clock Generator

Highlights

- Quick migration of 80186EC based designs to an FPGA platform
- Replacement for 80186EC processor and ASICs

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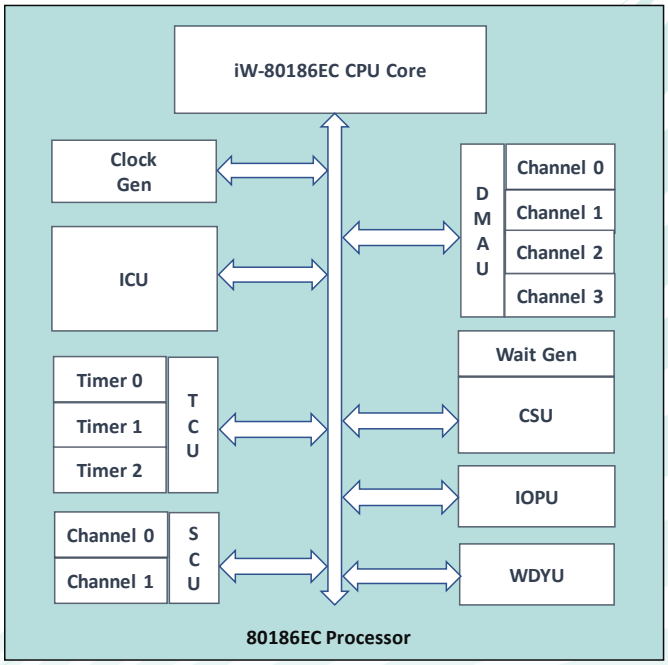
iW – 80186EC Processor IP block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
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iW- 80186EC Processor FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/80186ec-processor/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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